IPCLOCK

IPC9830

IEEE 1588 Boundary, Slave and Master Clock System on Chip DATASHEET

About the IPC9830

The IPC9830 is an IEEE 1588 boundary, slave and master clock, System on Chip, utilizes IPClock's state-of-the-art technology for providing high quality frequency synchronization and time of day (ToD) accuracy over packet transport networks (PTN). Clock synchronization is required by many wireline and wireless applications including 3G, 4G-LTE, Smart Grid, Industrial automation and aerospace and defense. The IPC9830 leverages Xilinx's XC6SLX45 Spartan-6 FPGA to provide application-agnostic, cost effective, reliable and standard compliant IEEE 1588 boundary, slave and master clock designed for enabling applications requiring accurate synchronization. The IPC9830 is designed for easy field upgrades and future enhancements support.

Main Features and Benefits

- Standalone IEEE 1588 v2 standard compliant boundary, slave and master clock System on Chip
- Excellent synchronization performance over most extreme packet transport network conditions
- Slave ToD alignment error is better than ±1µsec on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- Slave frequency accuracy performance is better than 16ppb on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- Adaptive to network impairments
- Provides precision holdover
- Slave meets 3G, 4G-LTE frequency and ToD accuracy
- Hybrid IEEE 1588/SyncE support. Requires external SyncE PLL.
- Supports up to 64 slaves/channels
- Supports Unicast/Multicast
- Supports one step / two steps
- Low total cost of ownership
- Zero touch approach can make external CPU redundant
- Easily integrates in existing and next generation designs
- Upgradeable by software
- Easy adding of enhancements and supporting emerging clock synchronization standards
- Operates with either TCXO or OCXO (10MHz, 12.8MHz or 20MHz)
- Interfacing generic PHY
- Master can lock to undisciplined 1PPS signal from GPS
- Standard compliant Best Master Clock (BMC) algorithm
- Modes of operation: Free run, Trace, Lock and Holdover
- Flexible reference clock input: 1PPS, 1.544MHz, 2.048MHz, or 10MHz
- Programmable clock outputs frequencies: 1.544MHz, 2.048MHz, or 10MHz
- Utilize Xilinx's Spartan 6 FPGA - XC6SLX45
- 324 pin BGA, 15 mm x 15 mm,0.8 mm pitch RoHS package

(*) The performance tested under the ITU-T G.8261 test suite provide an indication for IPClock's technology capabilities and is not guaranteed across all types of network elements and network conditions. Please contact IPClock's support for more information.

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1 Reference System Diagram

Figure 1 below depicts common network architecture including frequency and/or time of day (ToD) distribution over packet transport network using IEEE 1588 boundary, slave and master clock that may be integrated in each network element and in the Grandmaster.

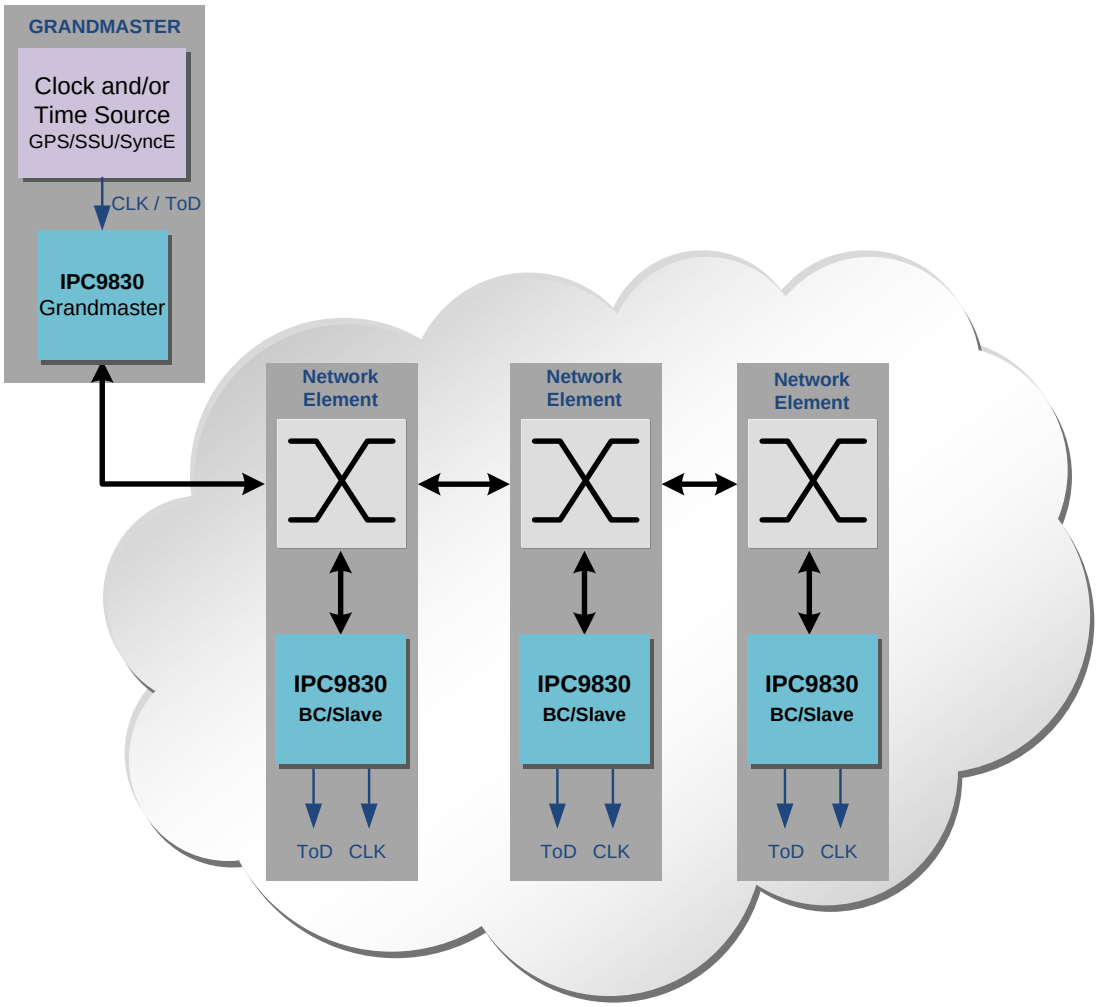


Figure 1: Accurate Time of Day, 1PPS and Frequency Distribution

The Grandmaster incorporates the IPC9830 in order to lock to a reference clock contains either 1PPS and ToD from a GPS receiver, or other clocks from other sources such as SSU. Each network element includes the IPC9830 uses for clock recovery, implementing IEEE 1588 standard compliant boundary or slave clock.

2 General Description

The IPC9830 is an IEEE 1588 standard compliant standalone boundary, slave and master clock System on Chip. The mode of operation (BC/Slave/Master) can be changed using the IPC9830 application-programming interface (API) functions. When set to work in BC and slave modes, the IPC9830 is synchronizing its real time clock to the master's real time clock. Powered by IPClock's state-of-the-art clock synchronization algorithms suite, the IPC9830 is capable of achieving cutting edge synchronization performance. IPClock's algorithm suite is capable of filtering out the impact of the packet transport network impairments on IEEE 1588 packets, which results packet delay variation, packet loss, packet duplication, and network re-route. The IPC9830 is an excellent choice for applications requiring precision clock synchronization.

For example, the IPC9830 can provide required timing for the following applications:

- Precision time of day and frequency synchronization for 3G, 4G-LTE and WiMAX cellular backhauling enabling cellular operators to migrate to a true all IP backhaul networks.
- Precision timing required by smart grid application and in particular by wide area protection, substation automation, and phasor measurement applications.
- Accurate frequency synchronization for circuit emulation services enabling reliable T1 or E1 transmission over packet switched network.

When set to work in BC/Master modes, the IPC9830 supports up to 64 slaves. The IPC9830 supports unicast and multicast operation.

Both master and slave have precision holdover allowing maintaining adequate clock synchronization in case reference clock signal is not available or degraded. In holdover, the clock synchronization performance dependents on the oscillator quality. Proper oscillator should be selected to meet the application's time-of-day and frequency accuracy requirements. The IPC9830 is supporting a variety of IPClock approved oscillators.

The IPC9830 includes all the functionality required for implementing a complete standalone IEEE 1588 BC/slave/master System on Chip including hardware assist functionality, e.g., timestamp generator, clock synchronization algorithms suit (also known as servo) and standard compliant IEEE 1588 protocol stack. It leverages Xilinx's XC6SLX45 Spartan-6 FPGA to provide application-agnostic, cost effective, reliable and standard compliant solution that can easily integrate into existing and next generation designs. Being a System on Chip the IPC9830 can be simply upgraded by downloading new configuration and/or software files allowing easy addition of enhancements as well as updates required for supporting emerging clock synchronization standards.

By default, the IPC9830 start operates as IEEE 1588 BC with no external configuration required once completing to download the IPC9830's hardware configuration and the software. Default configuration values can be modified using the IPC9830 application-programming interface (API) package for configuring as well as for controlling and monitoring the IPC9830. The APIs allow software developers to easily configure, control and monitor the IPC9830 providing the means for integrating the IPC9830 functionality into the code.
The IPC9830 is requiring 64MB of DDR2 memory and generic PHY supporting RGMII interface. The PHY address should be 8. Configuring the IPC9830 FPGA performed by 8MB SPI FLASH memory.

Oscillator minimal requirements: nominal frequency 20MHz, 12.8MHz or 10MHz free-run accuracy 4.6ppm, frequency stability over temperature range 50ppb, temperature range: -20 to 70', frequency slop: 2ppb/'C.

3 Functional Block Diagram

The IPC9830 functional block diagram is given in Figure 2 below.

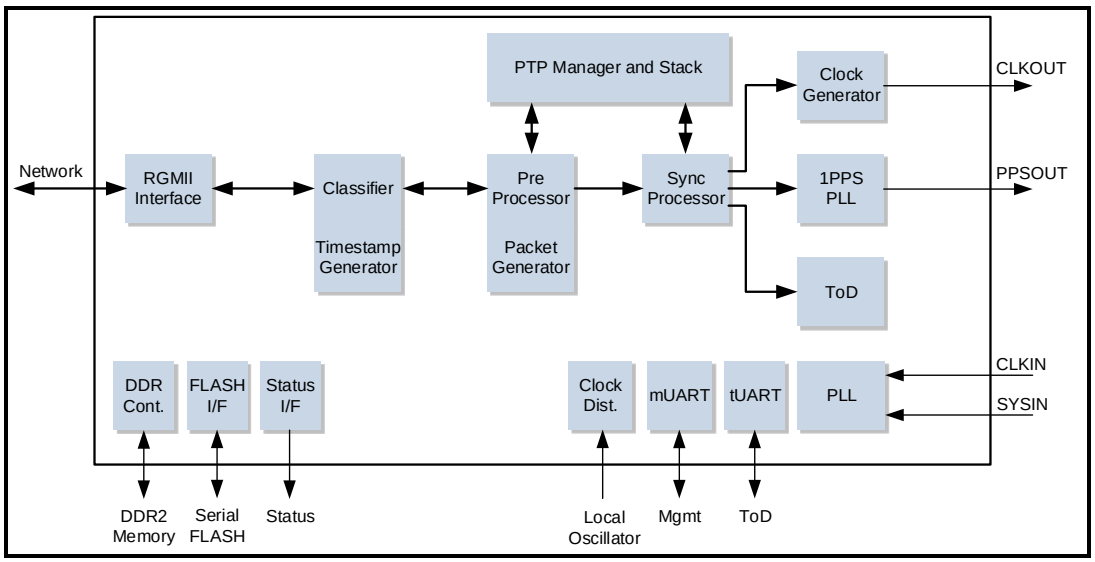


Figure 2: IPC9830 Functional Block Diagram

The IPC9830 can be set to operate as either IEEE 1588 BC or slave or master. The IEEE 1588 protocol is a bidirectional protocol requiring all ports to transmit and receive IEEE 1588 packets. Each packet received its time-stamp by the Timestamp Generator and classified by the Classifier. In the case the packet is IEEE 1588 packet it is sent to the Pre-Processor along with its timestamp. The Pre-Processor is transferring the received general packets to the PTP Manager and Stack for further processing. In the case of IEEE 1588 event packet the Pre-Processor compensate for part of the packet network impairments and prepare the data for the Sync Processor. The Sync Processor is comprised of a suite of algorithms that processes the data and controls the 1PPS PLL, the four programmable clock outputs of the Clock Generator, and the ToD. The ToD is communicating with the ToD UART utilizing the NMEA protocol for either providing or getting the ToD from a GPS. The IEEE 1588 packets are transmitted by the Packet Generator which is controlled by the PTP Manager and Stack. Each packet transmitted is time-stamped by the Timestamp Generator and this timestamp is either embedded into the packet or sent to the Pre-Processor depending on the packet type and selected mode of operation. The pull-in range of the BC, slave and master is complying with stratum 3 pull-in range as specify in GR1244.

4 Operational Description

The IPC9830 is providing applications with precision clock and time of day (ToD) synchronization over packet transport networks. The IPC9830 can be set to operate as either IEEE 1588 boundary clock (BC), slave or master.

The IEEE 1588 protocol is a bidirectional protocol requiring the BC, slave and master to transmit and receive IEEE 1588 packets. The packets exchange is used by the BC slave port or by the slave to calculate the delay to the selected master in order to align its real time clock to the master's real time clock. The calculations are based on measuring the roundtrip delay between the slave and the master. The measured roundtrip is divided by two to get the trip delay from the master to the slave.

The delay measurement calculations defined in the IEEE 1588 standard assume that networks are symmetrical. Any asymmetry between the path of the sync packets and the path of the delay request packets will cause an inherent offset to the slave's real time clock relative to the master's real time clock. There are many reasons for network asymmetries. Some of the network asymmetries can be compensated by implementing BC or transparent clock (TC) or a combination of both in the network. For example, the IPC9830 can be added to network elements to compensate for network asymmetry. In addition, adding BC functionality to network elements will reduce the amount of packet delay variation which will allow the IEEE 1588 slaves to improve their synchronization performance.

4.1 Administrative State Machine

The IPC9830 administrative state diagram is shown in Figure 3 below.

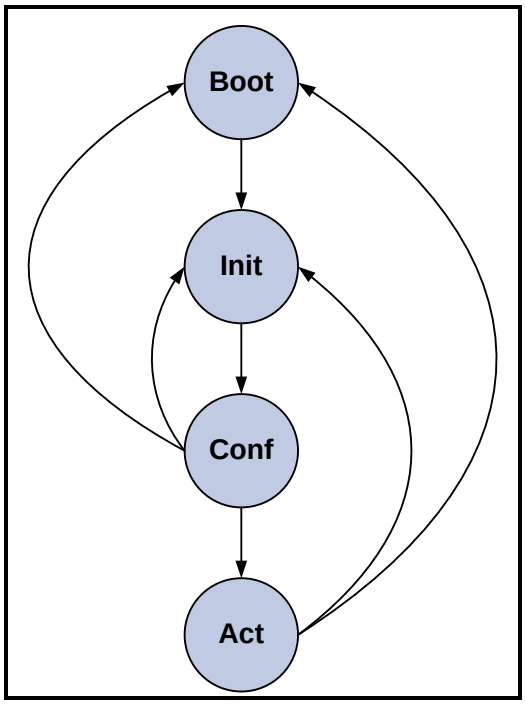


Figure 3: IPC9830 Administrative State Machine

After downloading the code into the IPC9830, it will enter the boot state. In this state, the IPC9830 is performing sanity tests like code integrity. The IPC9830 will continue to the init state upon successful completion of the tests in the boot state.

In the init state, the IPC9830 is preparing for operation by initializing internal software parameters and hardware registers. After initialization, the IPC9830 will perform the following tests:

- Reading known data from a pre-determined register
- Writing data to registers and reading back
- PLL lock state
- Valid clock in signal
- Successful initialization of the clock recovery algorithm and the protocol stack

The IPC9830 will continue to configuration (Conf) state upon successful completion of the Init state. In conf state, the IPC9830 is configuring the mode of operation according to the configuration parameters stored in FLASH memory or as default. The IPC9830 will repeat all tests made in the init state to validate configuration. In addition, the IPC9830 will perform configuration sanity test to make sure they are valid.

The IPC9830 will continue to the active (Act) state upon successful completion of the Conf state. In Act state, the IPC9830 invokes the IEEE 1588 application. By default, the IPC9830 is set to BC mode of operation.

The STATFR, STATHO, STATTR, STATLK, and STAT[1:0] pins are indicating the device status. The signal levels are shown in Table 1 below. 0 indicates Low, 1 indicates High, and X indicates Low or High.

	Boot	Init	Conf	Act
STATFR	0	0	0	X
STATHO	0	0	0	X
STATTR	0	0	0	X
STATLK	0	0	0	X
STAT[0]	0	0	0	X
STAT[1]	0	0	0	X

Table 1: Status Pins Levels

The pin status in active (Act) mode defined by the synchronization state machine as describes in the following chapters.

4.2 Operating as Boundary Clock

When set to operate as boundary clock (BC) the IPC9830 will have one port set to operate in Master mode and one in Slave mode. The Slave port could lock either to a grandmaster or to a Master port of another BC. The Master port could serve up to 64 slaves.

4.2.1 IPC9830 Slave Port Operation

When set to operate as BC, the IPC9830 Slave port will transmit delay request and signaling packets and will expect to receive sync, optionally follow up, delay response, announce and signaling packets.

The IPC9830 Slave port is requiring updating the unicast master table with the IEEE 1588 master IP addresses. Once this table is updated the IPC9830 Slave port will send request unicast transmission signaling (RUTS) for announce packets to all masters in the table.

Once receiving announce packets the IPC9830 Slave port invokes the best master clock (BMC) algorithm and builds a table containing a list of IEEE 1588 masters from which it chooses the master announced it is locked to the best accurate and stable reference clock. For example, a reference clock from GPS is considered a more accurate and stable reference clock than NTP. Once a master is selected, the IPC9830 Slave port will transmit request unicast transmission signaling (RUTS) packets for sync and delay response to the selected master. Unicast transmission of sync and Delay Response will eliminate asymmetry often caused by the way network elements are handling multicast packets.

The default sync rate and delay request rate can be modified via APIs though it is recommended to keep these values at their default values to accommodate severe network behavior that may degrade the synchronization performance if using lower sync and delay request packet rate. The IPC9830 Slave port can negotiate sync packet rates in the range of 2 to 128 in 2^N steps (N=1…7) and delay response packet rates of 1 every 16 seconds up to Sync packet rate.

The Slave port will remain locked to the master unless one (or more) of the following occur:

1. There is a new master locked to a better clock than the active master
2. The active master status had changed indicating lower quality than other masters
3. There is a disconnect between the slave and the master

Changes to the quality of the clock and the status of the master are carried by the announce packets sent by the master. In case 1 and case 2 the decision to lock to another master is based on the information carried in the announce packets. In the case announce packets are not received for a predefined threshold the slave port assumes that the master is not reachable and will attempt locking to a new master. In all three cases, the IPC9830 Slave port will attempt locking to the best master found in the master table.

4.2.2 IPC9830 Master Port Operation

The IPC9830 Master port communicates with a group of slaves belonging to the same master's domain. The logical connection between the Master port and its slaves is referred to as the communication path (commpath). The commpath is independent of the packet transport network's infrastructure connecting the Master to its slaves.

The Master port will transmit sync, follow up, delay response, announce, and signaling packets over UDP/IP in accordance with IEEE 1588 appendix D as unicast packets.

The trigger for start sending sync packets to a slave is by receiving a request unicast transmission signaling (RUTS) packet from a slave in the master's domain. This signaling message contains, amongst other things, the requested sync packet rate the requested commitment duration. The Master port will respond to the slave with a grant RUTS packet (GRUTS).

The GRUTS packet contains the actual sync packet rate allocated to the salve and the committed duration by which the IPC9830 Master port is to send Sync packets at the allocated rate. The IPC9830 Master port is supporting sync packet rates of 2^N (N=1…7) sync packets per second.

The IPC9830 includes mechanisms allowing early detection of connection loss to a slave it is serving. The early connection loss mechanism will trigger packet mute to a slave in case of connection loss to avoid packet flooding in the network. The IPC9830 will reserve the resources it allocated to a slave until either of the following conditions is met:

1. A slave was inactive for a time above a configurable threshold
2. A slave did not renew the unicast commitment
3. The slave was manually removed

4.2.3 BC Synchronization State Machine

In BC mode of operation, the Master port clock and time are provided directly by the Slave port hence the IPC9830 state is reflecting the state of the Slave port.

Figure 4 below depicts the IPC9830 synchronization state-machine when in BC mode.

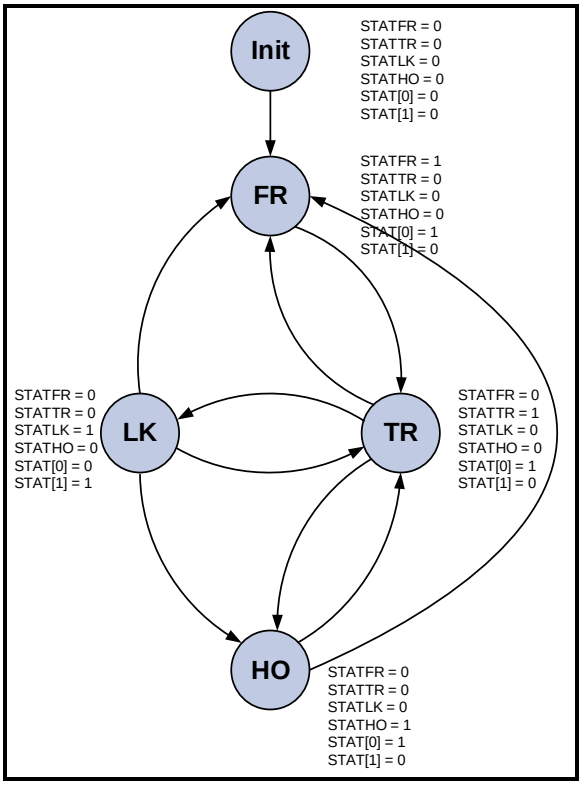


Figure 4: IPC9830 BC Synchronization State Machine

The IPC9830 BC starts in Init state. In this state, the IPC9830 BC is preparing for operating. Once completed, the IPC9830 BC will transition to free run (FR) state. The IPC9830 BC will transition to Trace (TR) state when a valid IEEE 1588 packet stream is detected by the Slave port. Valid IEEE 1588 packet stream defines as proper flow of Sync, FU (in two steps) and DelayResp packets.

In TR state, the IPC9830 BC is waiting for the Slave port to attempt locking to the master. If successful, the IPC9830 BC will transition to lock (LK) state. In case the IPC9830 Slave port was unable to lock to the master within 120 minutes, it will transition to free run (FR) state.

In case the Slave port lost the IEEE 1588 packet stream from its master the IPC9830 BC will transition to holdover (HO) either from LK state or from TR state. The IPC9830 BC will transition from HO to FR state in case the Slave port was in HO state for a consecutive 120 minutes. The IPC9830 BC will transition to TR state should the packet stream resumes to the Slave port.

Note *STATFR, STATTR, STATLK, and STATHO pins are indicating the IPC9830 PTP synchronization status (see Table 13 for more details).*

The table below summarizes the state transitions events.

Transition	Event
➔ Init	Power up.
Init ➔ FR	Initialization completed.
FR ➔ TR	Valid IEEE 1588 packet stream detected.
TR ➔ LK	Estimated phase error is within the defined threshold. The estimated phase error presented by ***slaveStateEx*** as reported by ***GetIpcPtpState*** API. The transition is determined by ***slaveStateEx*** and by ***slaveStateLkTh***, set by ***SetIpcPtpStateSlaveLkTh*** API. For additional information, refer to the User Guide, ***GetIpcPtpState*** and ***SetIpcPtpStateSlaveLkTh*** APIs.
TR ➔ HO	Valid IEEE 1588 packet stream lost, while ***slaveStateHoReady*** as reported by ***GetIpcPtpStateSlaveHoReady*** is greater than 0. For additional information, refer to the User Guide, ***GetIpcPtpStateSlaveHoReady*** and ***GetIpcPtpState*** APIs.
LK ➔ TR	Estimated phase error is exceeding the defined threshold. The estimated phase

Transition	Event
	error presented by ***slaveStateEx*** as reported by ***GetIpcPtpState*** API. The transition is determined by ***slaveStateEx*** and by ***slaveStateLkTh***, set by ***SetIpcPtpStateSlaveLkTh*** API. For additional information, refer to the User Guide, ***GetIpcPtpState*** and ***SetIpcPtpStateSlaveLkTh*** APIs.
LK ➔ HO	Valid IEEE 1588 packet stream lost, while ***slaveStateHoReady*** as reported by ***GetIpcPtpStateSlaveHoReady*** is greater than 0. For additional information, refer to the User Guide, ***GetIpcPtpStateSlaveHoReady*** and ***GetIpcPtpState*** APIs.
LK ➔ FR	Valid IEEE 1588 packet stream lost, while ***slaveStateHoReady*** as reported by ***GetIpcPtpStateSlaveHoReady*** is 0. For additional information, refer to the User Guide, ***GetIpcPtpStateSlaveHoReady*** and ***GetIpcPtpState*** APIs.
HO ➔ TR	Valid IEEE 1588 packet stream detected.
HO ➔ FR	Consecutive 120min in HO state.
TR ➔ FR	Valid IEEE 1588 packet stream lost, while ***slaveStateHoReady*** as reported by ***GetIpcPtpStateSlaveHoReady*** is 0, or in TR state for more than consecutive 120min. For additional information, refer to the User Guide, ***GetIpcPtpStateSlaveHoReady*** and ***GetIpcPtpState*** APIs.

Table 2: IPC9830 BC State Transition Events Table

Definitions:
Valid IEEE 1588 packet stream detected *- defined as detection of sequential series of 15 Sync/FU packets followed by one sec duration with one delay response packet or more.*
Valid IEEE 1588 packet stream lost *- defined while one of the following conditions met:*
(1) over one second without receiving any qualified sync/follow-up packet.
(2) over thirty seconds without receiving any qualified delay response packet.

4.3 Operating as Master Clock

When set to operate as Master, the IPC9830 communicates with a group of slaves belonging to the same master's domain. The logical connection between the Master and its slaves is referred to as the communication path (commpath). The commpath is independent of the packet transport network's infrastructure connecting the Master to its slaves.

The IPC9830 will transmit sync, follow up, delay response, announce, and signaling packets over UDP/IP in accordance with IEEE 1588 appendix D. The IPC9830 will send sync, optionally follow up, delay response, announce and signaling packets as unicast or it will transmit sync, optionally follow up and announce packets in multicast, delay request and delay response in unicast packets over UDP/IP in accordance with IEEE 1588 appendix D. Alternatively it can be operated in multicast.

The trigger for start sending sync packets to a slave is by receiving a request unicast transmission signaling (RUTS) packet from a slave in the master's domain. This signaling message contains, amongst other things, the requested sync packet rate the requested commitment duration. The IPC9830 will respond to the slave with a grant RUTS packet (GRUTS).

The GRUTS packet contains the actual sync packet rate allocated to the salve and the committed duration by which the IPC9830 is to send Sync packets at the allocated rate. The IPC9830 is supporting sync packet rates of 2^N (N=1…7) sync packets per second.

The IPC9830 includes mechanisms allowing early detection of connection loss to a slave it is serving. The early connection loss mechanism will trigger packet mute to a slave in case of connection loss to avoid packet flooding in the network. The IPC9830 will reserve the resources it allocated to a slave until either of the following conditions is met:

1. A slave was inactive for a time above a configurable threshold
2. A slave did not renew the unicast commitment
3. The slave was manually removed

4.3.1 Master Synchronization State Machine

The IPC9830 can lock to either 1PPS from a GPS receiver or to a reference clock when set to operate as Master. Figure 5 below depicts the IPC9830 synchronization state-machine when in Master mode.

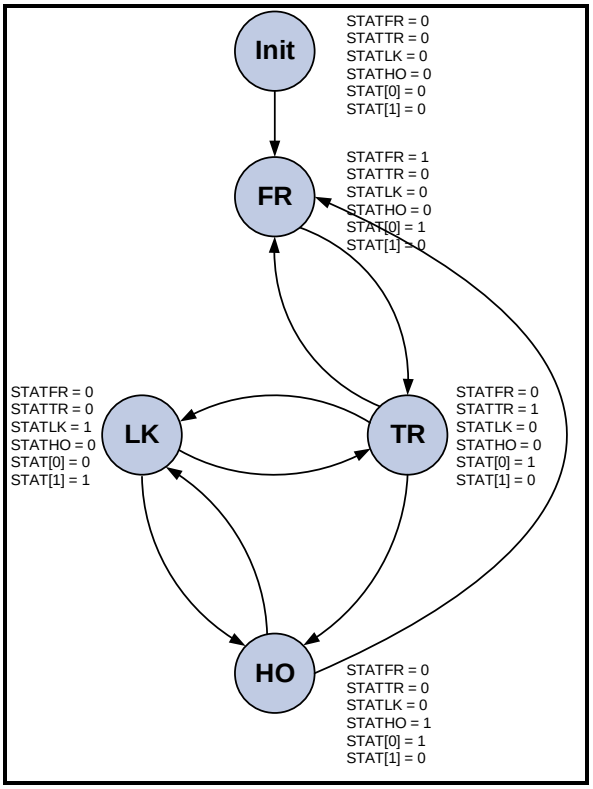


Figure 5: IPC9830 Master Synchronization State Machine

When set to operate as Master, the IPC9830 starts in Init state. In this state, the IPC9830 is preparing for operating as IEEE 1588 Master. Once completed, the Master will transition to free run (FR) state. The IPC9830 Master will transition to Trace (TR) state when a 1PPS signal or reference clock is detected (according to configuration).

In TR state the IPC9830 Master attempts locking to the 1PPS signal or reference clock. If successful, it will transition to lock (LK) state. In case the IPC9830 Master was unable to lock to the 1PPS signal or reference clock within 120 minutes, it will revert to free run (FR) state.

In case of 1PPS signal or reference clock loss, the IPC9830 Master will transition to holdover (HO) state either from LK state or TR state. The IPC9830 Master will transition from HO state to FR state in case it was in HO state for a consecutive 120 minutes. In case of 1PPS signal or reference clock resumed and is aligned with the device internal clock, the device will transition from HO to LK. In case of 1PPS signal or reference clock resumed and is not aligned with the device internal clock, the device will transition from HO to FR then TR, and in case lock conditions met, will transition to LK.

Note *STATFR, STATTR, STATLK, and STATHO pins are indicating the IPC9830 synchronization status (see Table 13 for more details).*

Table 3 below summarizes the state transitions events.

Transition	Event
➔ Init	Power up
Init ➔ FR	Initialization completed
FR ➔ TR	1PPS signal or reference detected
TR ➔ LK	Estimated phase synchronization performance is adequate(1)
TR ➔ HO	1PPS signal or reference clock is lost

Transition	Event
LK ➔ TR	Estimated phase synchronization performance is inadequate(1)
LK ➔ HO	1PPS signal or reference clock is lost
HO ➔ LK	1PPS signal or reference clock resumed and is aligned with the device internal clock
HO ➔ FR	Consecutive 120min in HO state OR 1PPS signal or reference clock resumed and is not aligned with the device internal clock
TR ➔ FR	Consecutive 120min in TR state

Table 3: IPC9830 Master State Transition Events Table

Note *(1) Adequate synchronization performance is defined as the estimated timing error ≤100ns*

4.4 Operating as Slave Clock

When set to operate as slave, the IPC9830 will transmit delay request and signaling packets. It will expect to receive sync, optionally follow up, delay response, announce and signaling packets. The IPC9830 expects to receive sync, optionally follow up, delay response, announce and signaling packets as unicast or sync, optionally follow up and announce packets in multicast, delay request, delay response and signaling packets in unicast.

The IPC9830 is requiring updating the unicast master table with the IEEE 1588 master IP addresses. Once this table is updated the IPC9830 will send request unicast transmission signaling (RUTS) for announce packets to all masters in the table. In multicast mode, the masters are automatically updated by receiving multicast announce packets from each active master.

Once receiving unicast or multicast announce packets the IPC9830 invokes the best master clock (BMC) algorithm and builds a table containing a list of IEEE 1588 masters from which it chooses the master announced it is locked to the best accurate and stable reference clock. For example, a reference clock from GPS is considered a more accurate and stable reference clock than NTP. Alternatively, a master can be selected manually using the APIs. Once a master is selected, the IPC9830 will transmit request unicast transmission signaling (RUTS) packets for sync and delay response to the selected master. Unicast transmission of sync and Delay Response will eliminate asymmetry often caused by the way network elements are handling multicast packets. In case of multicast mode, the slave will transmit RUTS for delay response only. Multicast transmission may cause asymmetry. However, this asymmetry can be reduced in a well-engineered network. The benefit of multicast is a lower bandwidth required for IEEE 1588 packets.

The default sync rate and delay request rate can be modified via APIs though it is strongly recommended to keep these values at their default values to accommodate severe network behavior that may degrade the synchronization performance if using lower sync and delay request packet rate. The IPC9830 can negotiate sync packet rates in the range of 2 to 128 in 2^N steps (N=1…7) and delay response packet rates of 1 every 16 seconds up to Sync packet rate.

The Slave will remain locked to the master unless one (or more) of the following occur:

1. There is a new master locked to a better clock than the active master
2. The active master status had changed indicating lower quality than other masters
3. There is a disconnect between the slave and the master

Changes to the quality of the clock and the status of the master are carried in the announce packets sent by the master. In case 1 and case 2 the decision to lock to another master is based on the information carried in the announce packets. In the case announce packets are not received for a predefined threshold the slave assumes that the master is not reachable and will attempt locking to a new master. In all three cases, the IPC9830 will attempt locking to the best master found in the master table hence providing inherent redundancy in case of active master failures or network disconnects. The time to declare a master as invalid is configurable and can be set via API.

The IPC9830 provides an extensive statistics and monitoring features including counters and network performance statistics including roundtrip delay, PDV measurements and PDV histograms. The IPC9830 network performance monitoring and statistics features provide a closer look to the network behavior.

4.4.1 Slave Synchronization State Machine

As described in chapter 4.2.3 - BC Synchronization State Machine.

5 Pin Diagram

Figure 6 below depicts the IPC9830 pin composition.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	PPSOUT	CLKA	STATFR	NC	NC	NC	NC	NC	SYSIN	ETH RXD3	ETH TXD1	ETH TXCLK	NC	CLKOUT3	TUTX	TCK	GND	A
B	VCCAUX	CLKOUT1	CLKINS	STATLK	VCCO	NC	GND	ETH RXCTL	ETH RXCLK	VCCO	ETH RXD2	ETH TXD3	GND	CLKOUT2	VCCO	TURX	VCCAUX	TMS	B
C	DDRVREF	PM0	GND	STATHO	NC	TURXS	NC	NC	NC	CLKIN	NC	NC	ETH TXCTL	MURX	NC	GND	NC	NC	C
D	DDRA9	DDRA8	DDRA11	HSWAPEN	GND	TUTXS	VCCO	CLKB	CLKC	GND	NC	NC	VCCO	MUTX	TDI	TDO	NC	NC	D
E	NC	VCCDDR	DDRWEn	NC	VCCAUX	NC	NC	NC	VCCAUX	VCCO	NC	NC	ETH TXD2	VCCAUX	GND	NC	VCCO	NC	E
F	DDRBA1	DDRBA0	DDRA4	DDRA10	NC	NC	NC	NC	ETH RXD1	NC	NC	NC	ETH TXD0	NC	NC	NC	NC	NC	F
G	DDRCLKn	GND	DDRCLK	VCCDDR	GND	DDRA12	VCCINT	NC	ETH RXD0	VCCAUX	NC	GND	NC	NC	VCCO	NC	GND	NC	G
H	DDRD5	DDRD4	DDRA6	DDRA5	DDRA2	DDRA7	DDRCKE	GND	VCCINT	GND	VCCINT	NC	NC	NC	NC	NC	NC	OSCIN	H
J	DDRD7	VCCDDR	DDRD6	GND	VCCDDR	DDRA1	DDRA0	VCCINT	GND	VCCINT	GND	VCCAUX	NC	VCCO	GND	NC	VCCO	NC	J
K	DDRD3	DDRD2	DDRLDM	DDRUDM	DDRCASn	DDRODT	VCCAUX	GND	VCCINT	GND	VCCINT	NC	NC	NC	NC	NC	NC	NC	K
L	DDRD1	DDRD0	DDRLDSn	DDRLDS	DDRRASn	PM1	DDRA3	VCCINT	GND	VCCINT	GND	NC	NC	NC	SYSINA	NC	NC	NC	L
M	DDRD9	GND	DDRD8	VCCDDR	DDRVREF	GND	VCCINT	NC	VCCAUX	NC	ETH MDC	VCCINT	NC	NC	VCCO	NC	GND	NC	M
N	DDRD11	DDRD10	DDRVREF	DDRRZQ	NC	NC	NC	NC	NC	NC	ETH MDIO	M1	GND	NC	NC	NC	NC	NC	N
P	DDRUDSn	DDRUDS	PM2	DDRZIO	VCCAUX	NC	NC	NC	VCCO	VCCAUX	NC	NC	NC	VCCAUX	NC	DOUT_ BUSY	NC	NC	P
R	GND	VCCDDR	NC	GND	NC	VCCO	NC	NC	GND	NC	NC	VCCO	D0_DIN_MISO_MISO1	GND	CCLK	SUSPEND	VCCO	GND	R
T	DDRD13	DDRD12	NC	NC	RDWR_B	NC	NC	NC	NC	NC	NC	PRDCT_ KEY	MOSI_ CSI_B_ MISO0	D1_MISO2	M0	GND	NC	NC	T
U	DDRD15	DDRD14	INIT_B	VCCO	NC	GND	NC	NC	VCCO	NC	NC	GND	NC	VCCO	STATTR	STAT1	NC	NC	U
V	GND	PRGRM_B	CSO_B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	D2_MISO3	RSTn	STAT0	DONE	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 6: IPC9830 Pin Composition

Interface groups are colored according to operational groups:

Ground
Power
DDR Memory
Conf./SPI FLASH
ETH
Reset
Local mgmt UART
Other
ToD UART
Clock In/Out
Status
JTAG
NC Not connected
Test / Reserved

6 Pin Description

This section provides information describing the pins in the IPC9830. The pins description is organized in tables. Each table provides information for specific interface or pins group. The following convention is used:

Symbol	Pin Ref	I/O	Type	Description
Pin Symbol	Pin location	I – Input O – Output O^T - Tristate I/O – Input/Output NC – Not Connect	T – LVCMOS33 (3.3V) S – SSTL18_II S^{Diff} – Differential SSTL18_II P – Power G – Ground	Short description

Note *LVCMOS33 output pins have 12mA drive and slow slew rate except Tx RGMII Ethernet pins that have 8mA drive and fast slew rate.*

6.1 Hardware Download Configuration Interfaces

This section describes the methods for downloading the bit stream file to the IPC9830. The bit stream file is programming the IPC9830 hardware.

Table 4 below defines the IPC9830 configuration interface's mode pins.

Symbol	Pin Ref	I/O	Type	Description
M1	N12	I	T	Pull-down (2.4 kΩ) or tied directly to ground.
M0	T15	I	T	Pull-up (2.4 kΩ) or tied directly to VCCO.

Table 4: Configuration Interface Mode Selection

Table 5 below defines the IPC9830 SPI FLASH configuration interface pins.

Symbol	Pin Ref	I/O	Type	Description
HSWAPEN	D4	I	T	When Low, enables I/O pull-ups before and during configuration 0: Pull-ups during configuration 1: No pull-up
SUSPEND	R16	I	T	Shall be tied to ground
MOSI_CSI_B_MISO0	T13(1)	I/O	T	Master IPC9830 Serial Data Output and Master IPC9830 Serial Data Input. Connect to the SPI flash Slave data output pin
D0_DIN_MISO_MISO1	R13(1)	I/O	T	Master IPC9830 Input Serial Data Input and Slave SPI flash output. Connect to SPI flash Slave data input pin
CSO_B	V3(1)	O	T	Master SPI Chip Select Output. Active Low. Connect to the SPI flash Slave Select input.
CCLK	R15(1)	I/O	T	Configuration clock. Connect to the SPI flash Slave clock input.
DOUT_BUSY	P16	O	T	Serial data output. Used in multi-FPGA daisy-chain configuration.
INIT_B	U3	I/O	T	Initialization indicator. Active Low. Goes Low at start of configuration during initialization memory clearing process. Released at the end of memory clearing, where mode pins are sampled.
DONE	V17	O	T	IPC9830 Configuration Done. Low during configuration. Goes High when the IPC9830 successfully completes configuration.
PRGRM_B	V2	I	T	Program IPC9830. Active Low. When asserted Low for 500 ns or longer, forces the IPC9830 to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins after PROGRAM_B returns High.

Table 5: SPI Configuration Interface Pin Description

Note *(1) These pins will be used during runtime allowing using single SPI FLASH memory for storing the IPC9830 bit stream, software, and configuration database.*

Table 6 below defines the IPC9830 JTAG configuration interface pins.

Symbol	Pin Ref	I/O	Type	Description
TDI	D15	I	T	Test Data In. This pin is the serial input to all JTAG instruction and data registers. TDI is applied into the JTAG registers on the rising edge of TCK
TDO	D16	O	T	Test Data Out. This pin is the serial output for all JTAG instruction and data registers. TDO changes state on the falling edge of TCK
TMS	B18	I	T	Test Mode Select. This pin determines the sequence of states through the TAP controller on the rising edge of TCK.
TCK	A17	I	T	Test Clock. This pin is the JTAG Test Clock.

Table 6: JTAG Configuration Interface Pin Description

6.2 Runtime Interfaces

This section provides the pin descriptions of interfaces in use during runtime. The interfaces' pin configurations are valid only after completing downloading the bit stream to the IPC9830.

Table 7 below defines the IPC9830 DDR2 memory interface pins.

Symbol	Pin Ref	I/O	Type	Description
DDRD0	L2	I/O	S	DDR2 data bus bit 0
DDRD1	L1	I/O	S	DDR2 data bus bit 1
DDRD2	K2	I/O	S	DDR2 data bus bit 2
DDRD3	K1	I/O	S	DDR2 data bus bit 3
DDRD4	H2	I/O	S	DDR2 data bus bit 4
DDRD5	H1	I/O	S	DDR2 data bus bit 5
DDRD6	J3	I/O	S	DDR2 data bus bit 6
DDRD7	J1	I/O	S	DDR2 data bus bit 7
DDRD8	M3	I/O	S	DDR2 data bus bit 8
DDRD9	M1	I/O	S	DDR2 data bus bit 9
DDRD10	N2	I/O	S	DDR2 data bus bit 10
DDRD11	N1	I/O	S	DDR2 data bus bit 11
DDRD12	T2	I/O	S	DDR2 data bus bit 12
DDRD13	T1	I/O	S	DDR2 data bus bit 13
DDRD14	U2	I/O	S	DDR2 data bus bit 14
DDRD15	U1	I/O	S	DDR2 data bus bit 15
DDRBA0	F2	O^T	S	DDR2 Bank Address bit 0
DDRBA1	F1	O^T	S	DDR2 Bank Address bit 1
DDRA0	J7	O^T	S	DDR2 address bus bit 0
DDRA1	J6	O^T	S	DDR2 address bus bit 1
DDRA2	H5	O^T	S	DDR2 address bus bit 2
DDRA3	L7	O^T	S	DDR2 address bus bit 3
DDRA4	F3	O^T	S	DDR2 address bus bit 4
DDRA5	H4	O^T	S	DDR2 address bus bit 5
DDRA6	H3	O^T	S	DDR2 address bus bit 6
DDRA7	H6	O^T	S	DDR2 address bus bit 7
DDRA8	D2	O^T	S	DDR2 address bus bit 8
DDRA9	D1	O^T	S	DDR2 address bus bit 9
DDRA10	F4	O^T	S	DDR2 address bus bit 10
DDRA11	D3	O^T	S	DDR2 address bus bit 11
DDRA12	G6	O^T	S	DDR2 address bus bit 12
DDRLDS	L4(1)	I/O	S^{Diff}	DDR2 data strobe for DDRD[7:0]
DDRLDSn	L3(2)	I/O	S^{Diff}	DDR2 data complement strobe for DDRD[7:0]
DDRUDS	P2(1)	I/O	S^{Diff}	DDR2 data strobe for DDRD[15:8]
DDRUDSn	P1(2)	I/O	S^{Diff}	DDR2 data complement strobe for DDRD[15:8]
DDRLDM	K3	O^T	S	DDR2 data mask for DDRD[7:0]
DDRUDM	K4	O^T	S	DDR2 data mask for DDRD[15:8]
DDRRASn	L5	O^T	S	DDR2 active-low row address strobe

Symbol	Pin Ref	I/O	Type	Description
DDRCASn	K5	O^T	S	DDR2 active-low column address strobe
DDRWEn	E3	O^T	S	DDR2 active-low write enable
DDRODT	K6(3)	O^T	S	DDR2 on-die termination control
DDRRZQ	N4	I/O	S	Connect to 100Ω pull-down resistor
DDRZIO	P4	I/O	S	NC
DDRCLK	G3	O^T	S^{Diff}	DDR2 clock
DDRCLKn	G1	O^T	S^{Diff}	DDR2 complement clock
DDRCKE	H7	O^T	S	DDR2 clock enable

Table 7: DDR2 Memory Interface Pin Description

Note

(1) This pin is connected to an internal pull-down resistor.
(2) This pin is connected to an internal pull-up resistor.
(3) ODT is terminated internally by a 50Ω resistor.

Table 8 below defines the IPC9830 SPI FLASH memory interface pins. Those pins are also included in the SPI Configuration Interface Pins.

Symbol	Pin Ref	I/O	Type	Description
MOSI_CSI_B_ MISO0	T13	O	T	IPC9830 serial data output. Connect to SPI FLASH data input pin
D0_DIN_MISO _MISO1	R13	I	T	IPC9830 serial data Input. Connect to SPI FLASH data input pin
CSO_B	V3	O	T	Master SPI Chip Select Output. Active Low. Connect to the SPI FLASH Slave Select input.
CCLK	R15	O	T	Configuration clock. Connect to the SPI FLASH clock input.

Table 8: SPI FLASH Interface Pin Description

Table 9 below defines the IPC9830 RGMII Ethernet interface pins.

Symbol	Pin Ref	I/O	Type	Description
ETHTXCLK	A13	O	T	RGMII transmit clock
ETHTXCTL	C13	O	T	RGMII TXEN on rising edge of ETHTXCLK and logical derivative of TXEN and TXERR on falling edge of ETHTXCLK
ETHTXD0	F13	O	T	RGMII transmit data bus bit 0
ETHTXD1	A12	O	T	RGMII transmit data bus bit 1
ETHTXD2	E13	O	T	RGMII transmit data bus bit 2
ETHTXD3	B12	O	T	RGMII transmit data bus bit 3
ETHRXCLK	B9	I	T	RGMII receive clock
ETHRXCTL	B8	I	T	RGMII RXDV on rising edge of ETHRXCLK and a logical derivative of RXDV and RXERR on falling edge of ETHRXCLK
ETHRXD0	G9	I	T	RGMII receive data bus bit 0
ETHRXD1	F9	I	T	RGMII receive data bus bit 1
ETHRXD2	B11	I	T	RGMII receive data bus bit 2
ETHRXD3	A11	I	T	RGMII receive data bus bit 3
ETHMDC	M11	O	T	PHY management data clock
ETHMDIO	N11(1)	I/O	T	PHY management data I/O

Table 9: RGMII Ethernet Interface Pin Description

Note

(1) The ETHMDIO signal is required to be synchronous with the ETHMDC clock signal.

Note

The Ethernet PHY address is 8.

Table 10 below defines the IPC9830 management UART interface pins.

Symbol	Pin Ref	I/O	Type	Description
MUTX	D14	O	T	Management UART transmit signal
MURX	C14	I	T	Management UART receive signal

Table 10: Management UART Interface Pin Description

Table 11 below defines the IPC9830 ToD UART interface pins.

Symbol	Pin Ref	I/O	Type	Description
TUTX	A16	O	T	ToD UART transmit signal
TURX	B16	I	T	ToD UART receive signal

Table 11: ToD UART Interface Pin Description

Table 12 below defines the IPC9830 clock interface & SyncE clock interface pins.

Symbol	Pin Ref	I/O	Type	Description
OSCIN	H18	I	T	IPClock approved oscillator input
CLKIN	C10	I	T	Reference clock input
CLKINS	B3	I	T	Clock input secondary of 1PPS for protection
SYSIN	A10	I	T	System clock input, 10MHz from SyncE PLL
PPSOUT	A2	O	T	One pulse per second output
CLKOUT1	B2	O	T	Clock output
CLKB	D8	O	T	Clock B output of 1PPS for protection (optional)

Table 12: Clock Interface & SyncE Clock Interface Pin Description

Table 13 below defines the IPC9830 status interface pins.

Symbol	Pin Ref	I/O	Type	Description
STATFR	A4	O	T	PTP free run status output
STATTR	U15	O	T	PTP trace status output
STATLK	B4	O	T	PTP lock status output
STATHO	C4	O	T	PTP holdover status output
STAT0	V16	O	T	General status output bit 0
STAT1	U16	O	T	General status output bit 1

Table 13: Status Interface Pin Description

Table 14 below defines the IPC9830 STAT[1:0] pins truth table.

STAT[1:0]		State
00	Fail:	IPC9830 is not operating as required
01	Alarm:	IPC9830 may not operate as required or it is not in lock state
10	Pass:	IPC9830 is operating as required and it is in lock state

Table 14: STAT[1:0] Pins Truth Table

Note *Additional information about the Status indications is available in the user guide.*

Table 15 below defines the IPC9830 reset pin.

Symbol	Pin Ref	I/O	Type	Description
RSTn	V15	I	T	Active-low chip reset

Table 15: Reset Pin Description

6.3 Power GND and NC pins

Table 16 below defines the IPC9830 power supply pins.

Symbol	Pin Ref	I/O	Type	Description
VCCO	B5, B10, B15, D7, D13, E10, E17, G15, J14, J17, M15, R17, P9, R6, R12, U4, U9, U14		P	Supply voltage for I/O
VCCAUX	B1, B17, E5, E9, E14, G10, J12, K7, M9, P5, P10, P14		P	Auxiliary supply voltage

Symbol	Pin Ref	I/O	Type	Description
VCCDDR	E2, G4, J2, J5, M4, R2		P	Supply voltage for DDR interface
DDRVREF	C1, M5, N3		P	DDR reference voltage
VCCINT	G7, H9, H11, J8, J10, K9, K11, L8, L10, M7, M12		P	Supply voltage for internal core

Table 16: Power Supply Pin Description

Table 17 below defines the IPC9830 ground pins.

Symbol	Pin Ref	I/O	Type	Description
GND	A1, A18, B7, B13, C3, C16, D5, D10, E15, G2. G5, G12, G17, H8, H10, J4, J9, J11, J15, K8, K10, L9, L11, M2, M6, M17, N13, R1, R4, R9, R14, R18, T16, U6, U12, V1, V18		G	Ground

Table 17: Ground Pin Description

Table 18 below defines the IPC9830 not-connected pins.

Symbol	Pin Ref	I/O	Type	Description
NC	A5, A6, A7, A8, A9, A14, B6, C5, C6, C7, C8, C9, C11, C12, C15, C17, C18, D6, D8, D11, D12, D17, D18, E1, E4, E6, E7, E8, E11, E12, E16, E18, F5, F6, F7, F8, F10, F11, F12, F14, F15, F16, F17, F18, G8, G11, G13, G14, G16, G18, H12, H13, H14, H15, H16, H17, J13, J16, J18, K12, K13, K14, K15, K16, K17, K18, L12, L13, L14, L16, L17, L18, M8, M10, M13, M14, M16, M18, N5, N6, N7, N8, N9, N10, N14, N15, N16, N17, N18, P6, P7, P8, P11, P12, P13, P15, P17, P18, R3, R5, R7, R8, R10, R11, T3, T4, T5 T6, T7, T8, T9, T10, T11, T12, T14, T17, T18, U5, U7, U8, U10, U11, U13, U17, U18, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14			Not connected.

Table 18: Not-connected Pin Description

Table 19 below defines the IPC9830 other interface pins.

Symbol	Pin Ref	I/O	Type	Description
PM0	C2	I	S	Connect to 4.7/10 KΩ pull-down resistor
PM1	L6	I	S	Connect to 4.7/10 KΩ pull-down resistor
PM2	P3	I	S	Connect to 4.7/10 KΩ pull-down resistor

Table 19: Other Pin Description

7 Interfaces Description

7.1 Hardware Configuration Interface

The hardware configuration interface enable to load the IPC9830 bit stream file. The M1 and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors (2.4 kΩ), or tied directly to ground or VCCO. The mode pins should not be toggled during or before configuration. The IPC9830 hardware configuration bit stream file could be loaded from serial SPI Flash memory device. Compatible SPI FLASH memory device supported by the IPC9830 is Micron 8MB N25Q064A13ESE40.

7.2 SPI FLASH Memory

The SPI FLASH memory is used for downloading the IPC9830 hardware configuration and software as well as for storing/recalling the IPC9830 configuration database.

7.3 DDR2 Memory Interface

The IPC9830 is supporting 16-bit DDR2 memory devices. Compatible DDR2 memory device supported by the IPC9830 is Micron 64MB MT47H32M16HR-25E.

7.4 Ethernet RGMII Interface

The RGMII interface is commonly used to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins only. The data paths and all associated control signals are reduced and control signals are multiplexed together and both edges of the clock are used. For Gigabit operation, the clocks are operating at 125MHz, and for 100 Mbps operation, the clocks are operating at 25MHz.
Multiplexing of data and control is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the rising edge and the upper 4 bits on the falling edge. Control signals are multiplexed into a single clock cycle using the same technique.

7.4.1 RGMII Interface Functional Diagrams

Figure 7 below depicts RGMII interface transmit functional diagram.

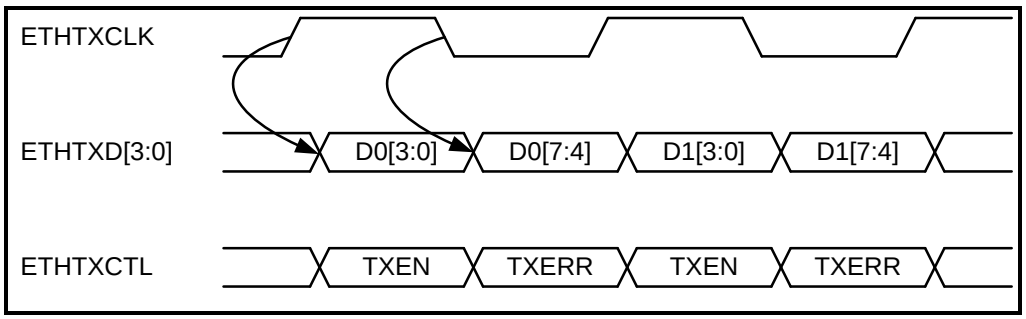


Figure 7: RGMII Interface Transmit Functional Diagram

As can be seen, the bits 3:0 of the first byte D0 are transmitted with the clock's rising edge whereas bits 7:4 of the first byte D0 are transmitted with the clock's falling edge. Note that TXEN is sampled with the clock's rising edge while TXEN XOR TXERR is sampled with the ETHTXCLK clock's falling edge.

Figure 8 below depicts RGMII interface receive functional diagram.

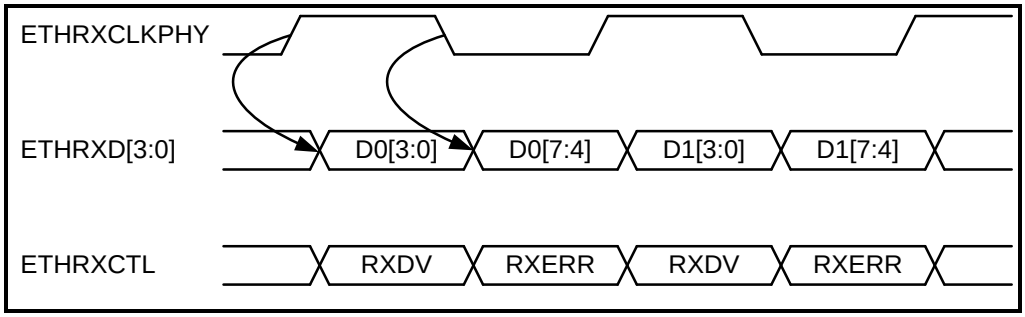


Figure 8: RGMII Interface Receive Functional Diagram

As can be seen, the bits 3:0 of the first byte D0 are read with the clock's rising edge whereas bits 7:4 of D0 are read with the clock's falling edge. Note that RXDV is sampled with the clock's rising edge while RXDV XOR RXERR is sampled with the ETHRXCLK clock's falling edge.

7.4.2 RGMII Interface Timing Diagrams

Figure 9 below provides the RGMII interface transmit timing diagram.

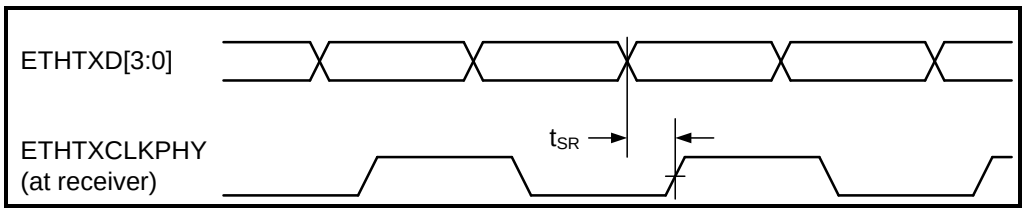


Figure 9: RGMII Interface Transmit Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{SR}	Data to clock output skew at receiver (PHY)	1		2.6	ns
$t_{ETHTXCLK}$	TXCLK cycle time		8		ns
t_{ETHDC}	1000Base-T duty cycle	45	50	55	%
$t_{ETHFEDC}$	100Base-TX duty cycle	40	50	60	%

Table 20: RGMII Interface Transmit Timing Data

The current limit of the clock and Data signals is 8mA.

Figure 10 below provides the RGMII interface receive timing diagram.

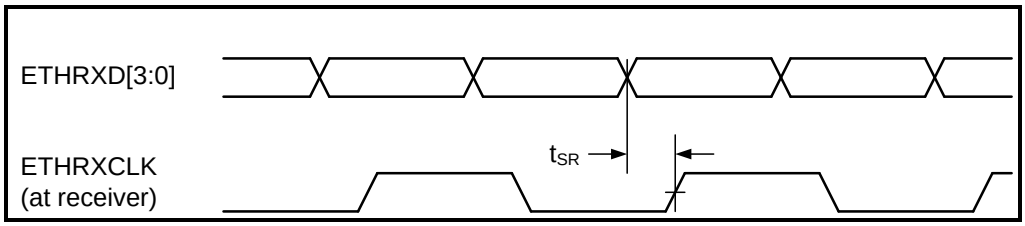


Figure 10: RGMII Interface Receive Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{SR}	Data to clock output skew at receiver (IPC9830)	-0.2		2.0	ns
$t_{ETHRXCLK}$	RXCLKPHY cycle time	7.2		8.8	ns
t_{ETHDC}	1000Base-T duty cycle	45		55	%
$t_{ETHFEDC}$	100Base-TX duty cycle	40		60	%

Table 21: RGMII Interface Receive Timing Data

7.4.3 PHY Management Interface Timing Diagram

Figure 11 below depicts the PHY management interface timing diagram.

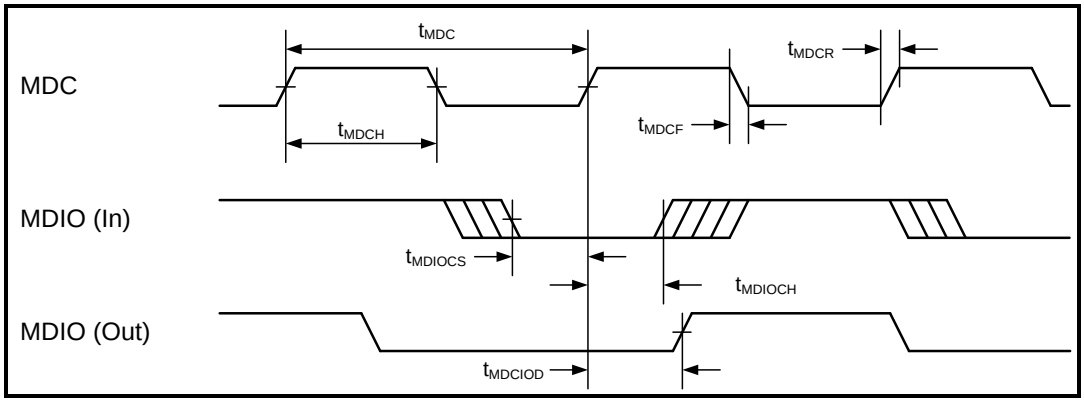


Figure 11: PHY Management Interface Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
f_{MDC}	MDC frequency		1.67		MHz
t_{MDC}	MDC period		600		ns
t_{MDCH}	MDC clock high pulse width		300		ns
t_{MDCIOD}	MDC to MDIO out delay			45	ns
t_{MDIOCS}	MDIO to MDC setup time	5			ns
t_{MDIOCH}	MDIO to MDC hold time	0			ns
t_{MDCR}	MDC rise time			10	ns
t_{MDCF}	MDC fall time			10	ns

Table 22: PHY Management Interface Timing Data

7.5 Local Management UART Interface

The mUART interface is for locally configure, control, and monitor the IPC9830 either by external CPU UART interface or from local terminal. The mUART is using standard non-return-to-zero (NRZ) format and is configured to 115,200 baud, 8 bits, No parity, and 1 stop bit.

7.6 Time of Day Interface

The Time of Day interface is comprised of a 1PPS signal and the Time of Day UART providing the NMEA GPRMC message.

Note *The ToD UART will send NMEA messages when in BC or Slave modes only if time is above GPS epoch, i.e., time in parent master is above GPS epoch.*

7.6.1 Time of Day UART

The tUART interface is for setting or getting the time-of-day from the IPC9830. When set to operate as IEEE 1588 Master, tUART is for setting the master time-of-day. When set to operate as IEEE 1588 BC or Slave, tUART is for getting the time-of-day from the IPC9830. The tUART is using standard non-return-to-zero (NRZ) format and is configured to 9,600 baud, 8 bits, No parity, and 1 stop bit.

7.6.2 The GPRMC Message Format

The global positioning recommended minimum data (GPRMC) message is a standard national marine electronics association (NMEA) message that provides, amongst other things, UTC date and time. The GPRMC message is supported by all GPS receivers.
When set to Master mode of operation, the IPC9830 is extracting the value from UTC Time field to update the current time. When set to BC or Slave mode of operation, the IPC9830 is transmitting GPRMC messages.

The IPC9830 GPRMC output message (62 bytes) format is given in the following example:

$GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0,0.0,110615,,,A*61

The IPC9830 supports two GPRMC input messages formats:

$GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0,0.0,110615,,,A*61
$GPRMC,122356.00,A,3523.414,N,13932.106,W,,,110615,,,A*44

The IPC9830 GPRMC output message is described in Table 23 below.

Field	Description
Message ID	$GPRMC
UTC Time	122356 (hh:mm:ss)
Status	A – Data valid or V – Data invalid
Latitude	0000.0000 (fixed to zero)
N/S Indicator	N- North
Longitude	0000.0000 (fixed to zero)
E/W Indicator	W – West
Speed over Ground	0.0 (fixed to zero)
Course over Ground	0.0 (fixed to zero)
UTC Date	110615 (ddmmyy)
Magnetic Variation	Empty
Direction of Variation	Empty
Mode	A = autonomous
Checksum	*61

Table 23: GPRMC Output Message Format using tUART

7.6.3 Timing Diagrams

The ToD input is comprised of the tUART TURX pin and a reference PPS signal connected to CLKIN pin. Figure 12 below depicts the TURX and CLKIN signals timing.

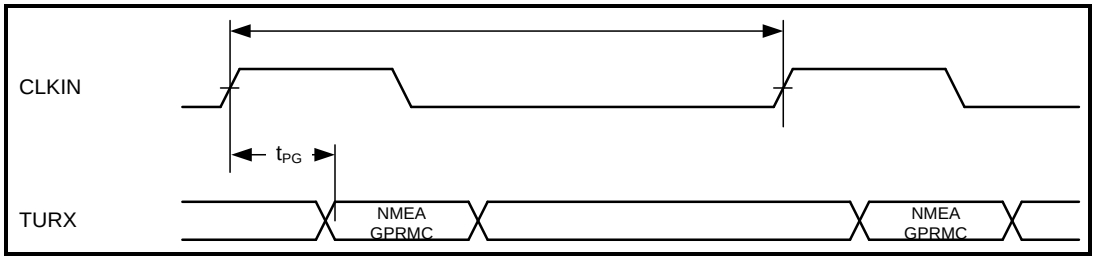


Figure 12: CLKIN and TURX Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{PG}	Time between PPSIN rising edge and GPRMC message	0.5		200	ms

Table 24: CLKIN and TURX Timing Table

The ToD output is comprised of the tUART TUTX pin and the PPSOUT pin. Figure 13 below depicts the TUTX and PPSOUT signals timing.

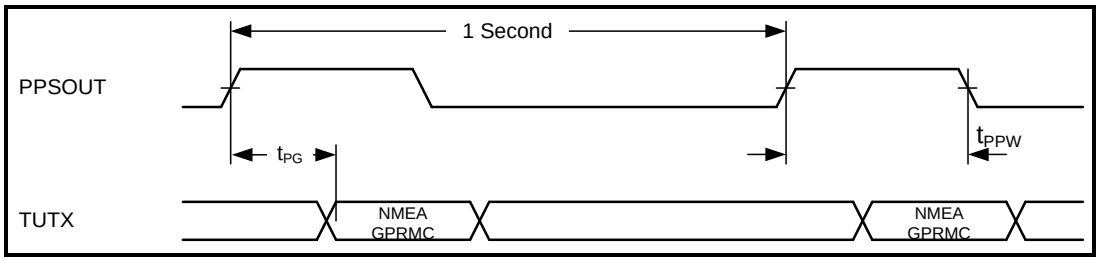


Figure 13: PPSOUT and TUTX Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{PG}	Time between PPSOUT rising edge and GPRMC message	0.5		200	ms
t_{PPW}	PPSOUT pulse width	200	250	300	ms

Table 25: PPSOUT and TUTX Timing Table

The 10 MHz clock out signal is phase aligned with the PPSOUT. Figure 14 below depicts the 10 MHz clock out and PPSOUT signals timing.

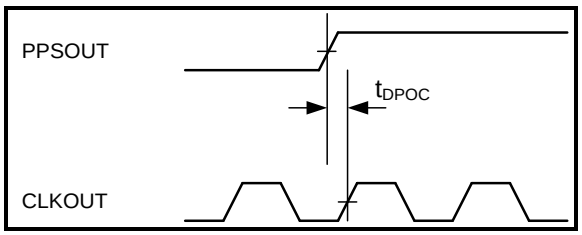


Figure 14: PPSOUT and 10 MHz Clock Out Phase Alignment

Symbol	Definition	Min	Typ	Max	Units
t_{DPOC}	Delay from PPSOUT rising edge and CLKOUT rising edge	-100		100	ns

Table 26: PPSOUT and CLKOUT Timing Table

7.7 Oscillator Input

The IPC9830 require using IPClock approved (or better) oscillators. The IPC9830 is supporting the following oscillator frequencies:

- 10MHz
- 12.8MHz
- 20MHz

The oscillator is connected to OSCIN pin. Alternatively, low-jitter system (WAN) PLL can drive the OSCIN. OSCIN signals must be valid under all conditions. In case OSCIN will not be valid during IPC9830 operation, the IPC9830 must be reset.

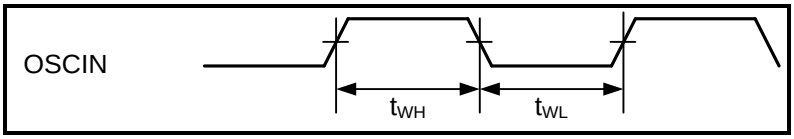


Figure 15: OSCIN Clock Signal

Symbol	Definition	Min	Typ	Max	Units
t_{WH}/t_{WL}	Duty cycle	45		55	%

Table 27: OSCIN Timing

7.8 Clock Interface

The IPC9830 clock interfaces support wide variety of operation modes such as IEEE 1588 BC, Master, Slave, Hybrid. In Hybrid mode, it can operate with external SyncE PLL.
The CLKIN is been used for reference clock input. PPSOUT provides the 1PPS signal and the CLKOUT1 provides 1544 KHz / 2048 KHz / 10 MHz clock.
The SYSIN pin can be used for Hybrid operation. Device uses SYSIN pin, if valid clock, as reference clock, and OSCIN pin for device operation. In case SYSIN clock is not valid, the device uses OSCIN as reference clock as well. The clock provided to SYSIN pin shall be IPClock approved (or better) oscillator or the output of low-jitter system (WAN) PLL.
The CLKINS pin, can be used for feeding 1PPS to the device from other sources. As an example, in master mode, the user can select CLKIN or CLKINS as the clock used by the master. In addition, in BC/Slave/Master modes, the user can select the PPSOUT clock source, it can be the internal clock (IEEE 1588 clock) or CLKIN or CLKINS.

7.9 Reset

The IPC9830 will be set to Init administrative state when asserting the RST signal.

Note *Complete reset requires reloading configuration to the IPC9830 (See section 7.1)*

7.9.1 Timing Diagram

Figure 16 below depicts the RSTn signal timing.

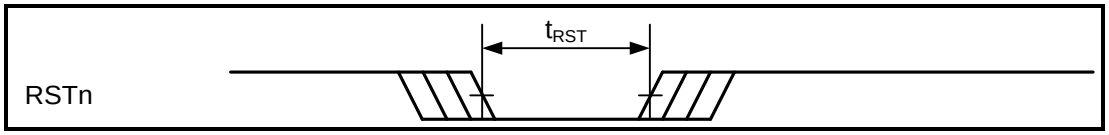


Figure 16: Reset Timing

Symbol	Definition	Min	Typ	Max	Units
t_{RST}	Reset assertion time	500			ns

Table 28: RST Timing Table

8 Electrical Specifications

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CCO}	Supply voltage for I/O	-0.5	3.75	V
V_{CCAUX}	Supply voltage for I/O	-0.5	3.75	V
V_{CCDDR}	Supply voltage for DDR interface, 1.8 V	-0.5	3.75	V
V_{CCINT}	Supply voltage for internal core, 1.2 V	-0.5	1.32	V
V_{IN}	I/O input voltage	-0.6	4.10	V
V_{OUT}	I/O output voltage	-0.5	V_{CCO}	V
T_{OP}	Operating temperature	-40	+85	°C
$T_{STORAGE}$	Storage temperature	-65	+150	°C
T_{SOL}	Soldering temperature		+260	°C

Table 29: Absolute Maximum Ratings

8.2 Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CCO}, V_{CCAUX}	Supply voltage for I/O, 3.3 V	3.15	3.3	3.45	V
V_{CCDDR}	Supply voltage for DDR interface, 1.8 V	1.70	1.8	1.90	V
V_{CCINT}	Supply voltage for internal core, 1.2 V	1.14	1.2	1.26	V
V_{IN}	I/O input voltage	-0.6		4.10	V
V_{OUT}	I/O output voltage	-0.5		V_{CCO}+0.5	V
P_{D33}	Power consumption for 3.3 V		1.0	1.1	W
P_{D18}	Power consumption for 1.8 V		1.0	1.2	W
P_{D12}	Power consumption for 1.2 V		0.8	1.0	W
T_{OPR}	Ambient operating temperature	-40		+85	°C

Table 30: Operating Conditions

8.3 Power Supply Ramp Time

Symbol	Parameter	Min	Typ	Max	Units
V_{CCO}	Supply voltage for I/O	0.20		50	ms
V_{CCAUX}	Supply voltage for I/O	0.20		50	ms
V_{CCDDR}	Supply voltage for DDR interface	0.20		50	ms
V_{CCINT}	Supply voltage for internal core	0.20		50	ms

Table 31: Power Supply Ramp Time

8.4 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{TINL}	I/O V_{IN} low	-0.5		0.8	V
V_{TINH}	I/O V_{IN} high	2.0		4.1	V
V_{TOL}	I/O V_{OUT} low			0.4	V

V_{TOH}	I/O V_{OUT} high	V_{CCO}-0.4		V
V_{SINL}	DDR I/O V_{IN} low	-0.5	0.38	V
V_{SINH}	DDR I/O V_{IN} high	0.8	4.1	V
V_{SOL}	DDR I/O V_{OUT} low		0.45	V
V_{SOH}	DDR I/O V_{OUT} high	V_{CCDDR}-0.45		V

Table 32: DC Characteristics

8.5 Electrical Protection

8.5.1 ESD Protection

The IPC9830 encompasses a protection against electrostatic discharge (ESD) input levels of up to ±2000 V in human body model (HBM) and up to ±500 V in charged device model (CDM) for all pins.

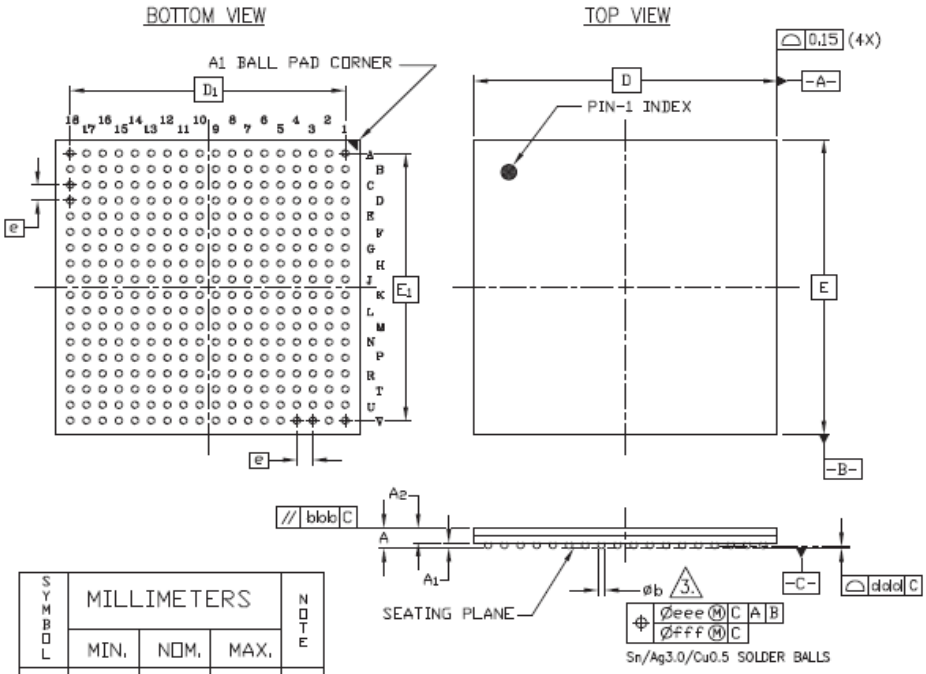
ESD results are obtained according to the following industrial standard specifications:

- HBM: ANSI/ESDA/JEDEC JS-001-2010
- CDM: JESD22-C101

8.5.2 Latchup Protection

The IPC9830 is protected against latchup input currents of up to ±200 mA and 1.5xVDD at 125°C. Latch-up results are obtained according to EIA/JESD78 specification.

9 Package Information



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.50	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.40	0.45	0.50	3
bbb			0.20	
ddd			0.20	
eee			0.15	
fff			0.08	
M	18			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE
5. CONFORMS TO JEDEC MO–275–KKAB–1

Figure 17: IPC9830 Package Information

10 Ordering Information

Part Number	Description
IPC9830-10	IEEE 1588 BC/Slave/Master System on Chip – Oscillator frequency: 10MHz
IPC9830-12	IEEE 1588 BC/Slave/Master System on Chip – Oscillator frequency: 12.8MHz
IPC9830-20	IEEE 1588 BC/Slave/Master System on Chip – Oscillator frequency: 20MHz

11 Contact Information

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