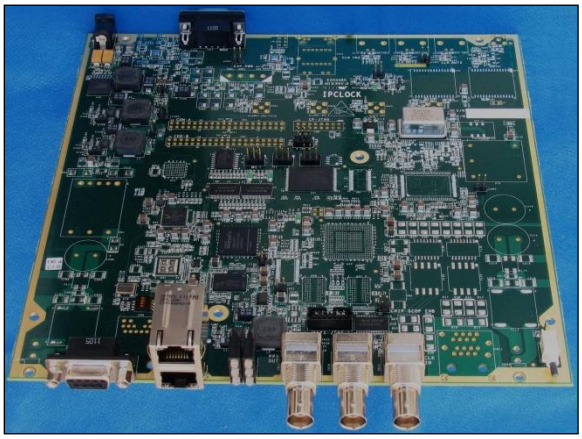
IPCLOCK
InSync

IPC300 EVB

IEEE1588v2 (PTP) Boundary Clock (BC) & Master / Slave Clocks



Features

- IEEE1588v2 BC and/or Master and/or Slave
- Best Master Clock (BMC) algorithm
- ToD alignment error is better than ±1µsec on a network comprised of 10-switch GbE network under G.8261 conditions(*)
- Frequency error is better than 16ppb on a network comprised of 10-switch GbE network under G.8261 conditions(*)
- Upgradable by software

Benefits

- Enable simple and fast PTP evaluation
- Simple setup and configuration
- Meeting LTE, UMTS, GSM/GPRS/EDGE, TD-SCDMA synchronization requirements

(*) The performance tested under the ITU-T G.8261 tests suite provide an indication for IPClock's technology capabilities and is not guaranteed across all types of network elements and networks conditions. Please contact IPClock's support for more information.

Product Overview

The IPC300 IEEE1588v2 Boundary and Master/Slave Clock enables equipment vendors and ASIC vendors to evaluate the IPC9000, IPC1710, IPC1603 chip on FPGA.

The IPC9000/IPC1710/IPC1603 is optimized for providing high quality frequency synchronization, phase alignment and accurate Time of Day (ToD) distribution over packet switched networks with the flexibility to operate either as PTP BC and/or Master and/or Slave.

With the IPC9000/IPC1710/IPC1603, the use of PTP is allowing leveraging the IP network for distributing the clock to the clients hence lowering the total network deployment and maintenance expenditures by reducing the number of GPS receivers to the minimum required.

The IPC300 incorporates IPClock's state-of-the-art IPC9000/IPC1710/IPC1603 designed to meet packet switched networks inherent impairments with proved excellent clock synchronization performance.

Typical applications for IPC9000/IPC1710/IPC1603 include:

- Telecom
- Cellular IP backhauling
- Aerospace and defense
- Smart Grid
- Homeland security
- Passive Optical Networks (PON)

IPC300 Specifications

Clock Interfaces

CLK IN

1PPS from GPS (non disciplined)
- Duty cycle: 20% to 60%
- Signal Level: HCMOS/TTL
- Connector: BNC 50Ω, female

1.544MHz, 2.048MHz, 10MHz
- Duty cycle: 40% to 60%
- Signal Level: HCMOS/TTL
- Connector: BNC 50Ω, female

CLK OUT

1.544MHz, 2.048MHz, 10MHz
- Duty cycle: 40% to 60%
- Signal Level: HCMOS/TTL
- Connector: BNC 50Ω, female
- Frequency accuracy (Slave): ≤16ppb (in lock state)
- G.823/G.824 sync interface compliant (Slave)

PPS OUT

1PPS
- Duty cycle: 20% to 60%
- Signal Level: HCMOS/TTL
- Connector: BNC 50Ω, female
- Phase lock accuracy (Slave): ≤1μsec (in lock state)
- Lock time: ≤900sec

TOD

TOD In / Out

ToD Message Protocol: NMEA
Connector: RS-232, 9-pin, D-type male

Network Interface

100/1000 ETH

100/1000 Base-T Ethernet
Connector: RJ-45

Management and Control

CLI based configuration and management
RS-232
Connector: 9-pin, D-type male

IEEE1588v2

IEEE1588v2 PTP
G.8265.1
G.8275.1
Boundary Clock
Master / Slave
Unicast / Multicast
ITU-T G.8261 compliant

LEDs

PWR: Power
STAT: Status
LK/TR: Lock/Trace
HO: Holdover
FR: Free Run

Power Requirements

Supply voltage: 9VDC
Power: 30W max

Environmental Conditions

Operating temperature: -0°C to +50°C
Storage temperature: -40°C to +85°C
Operating humidity: 5% to 95% (non condensing)

RoHS

2002/95/EC as amended by 2005/717/EC, 2005/747/EC, and 2005/618/EC

Physical Specifications

W×D (mm): 210 × 206
W×D (inch): 8.26 × 8.11