IPCLOCK
InSync

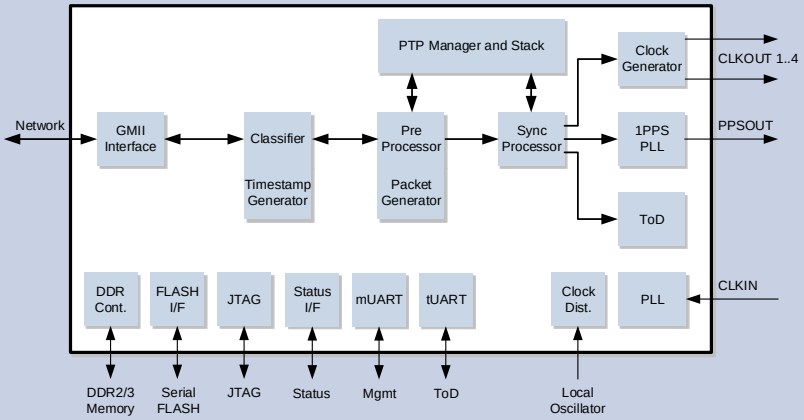
IPC9004

IEEE 1588 v2 Boundary Clock and Ordinary Clock IP Core

About IPC9004

The IPC9004 utilizes IPClock's state-of-the-art technology for IEEE 1588 v2 optimized for providing high quality frequency synchronization and Time of Day (ToD) over packet switched networks. Clock synchronization is required by many applications. For example, UMTS-FDD and Pseudo-wire (E1/T1) require the synchronization of frequency while LTE, WiMAX, CDMA2000 and GPS replacement require frequency synchronization, phase alignment and accurate Time of Day (ToD). The IPC9004 is IP core leveraging Xilinx® 7 series FPGAs. The IPC9004 is an application-agnostic, cost effective, reliable and standard compliant IEEE 1588 v2 BC and OC designed for enabling applications requiring high synchronization level. The IPC9004 is designed for easy field upgrades to support future enhancements as well as future clock synchronization standards.

IPC9004 Functional Block Diagram



The IPC9004 can be set to operate as either IEEE 1588 v2 Boundary Clock or Ordinary Clock master or Ordinary Clock slave. The IEEE 1588 v2 protocol is a bidirectional protocol requiring all ports to transmit and receive 1588 v2 packets. Each packet received its time-stamp by the Timestamp Generator and classified by the Classifier. In the case the packet is 1588 v2 packet it is sent to the Pre-Processor along with its timestamp. The Pre-Processor is transferring the received general packets to the PTP Manager and Stack for further processing. In the case of 1588 v2 event packet the Pre-Processor compensate for part of the packet network impairments and prepare the data for the Sync Processor. The Sync Processor is comprised of a suite of algorithms that processes the data and controls the 1PPS PLL, the programmable clock output of the Clock Generator, and the ToD. The ToD is communicating with the ToD UART utilizing the NMEA protocol for either providing or getting the ToD from a GPS. The 1588 v2 packets are transmitted by the Packet Generator which is controlled by the PTP Manager and Stack. Each packet transmitted is time-stamped by the Timestamp Generator and this timestamp is either embedded into the packet or sent to the Pre-Processor depending on the packet type and selected mode of operation.

Main Features and Benefits

- IEEE 1588 v2 compliant Boundary Clock and Master/Slave Ordinary Clock IP core
- ToD error is better than ±1µsec on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- Frequency accuracy performance is better than 16ppb on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- Standard compliant Best Master Clock (BMC) algorithm
- Supports up to 64 slaves/channels
- Flexible reference clock input: 1PPS, 1.544MHz, 2.048MHz, 10MHz, or 25MHz
- clock output: 8KHz, 1.544MHz, 2.048MH, or 10MHz
- Modes of operation: Free run, Trace, Lock, and Holdover
- Hybrid 1588/SyncE mode support
- Upgradeable by software
- Operates with either TCXO or OCXO (10MHz, 12.8MHz, or 20MHz)
- Interfacing generic PHY
- Low total cost of ownership
- Zero touch approach can make external CPU redundant
- Excellent performance with low cost oscillator
- Easily integrates in existing and next generation designs
- Provides excellent synchronization performance over most extreme packet transport network conditions
- Provides precision holdover
- Master can lock to undisciplined 1PPS signal from GPS
- Easy adding of enhancements and supporting emerging clock synchronization standards

(*) The performance tested under the ITU-T G.8261 tests suite provide an indication for IPClock's technology capabilities and is not guaranteed across all types of network elements and networks conditions. Please contact IPClock's support for more information.

Typical Application Example: Master, Boundary & Slave Clocks for Cellular Backhauling