IPCLOCK
InSync

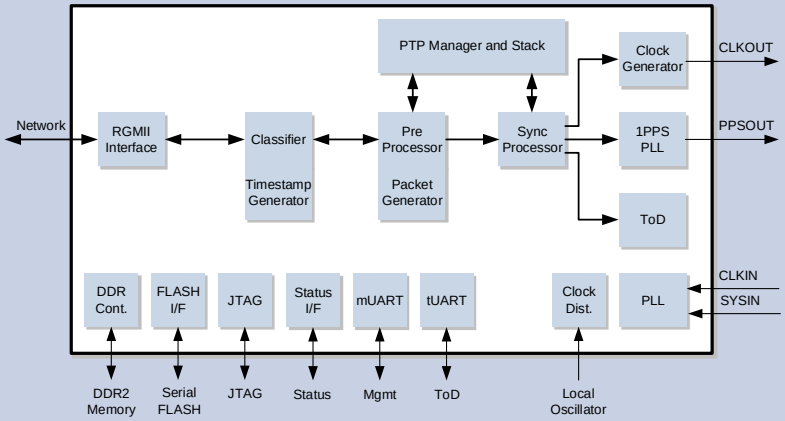
IPC1710

IEEE 1588 Master and Slave Chip on FPGA

About IPC1710

The IPC1710 utilizes IPClock's state-of-the-art IEEE 1588 v2 technology optimized for providing high quality frequency synchronization and Time of Day (ToD) over packet transport networks. Clock synchronization is required by many wireline and wireless applications including 3G, 4G-LTE, 5G, smart grid, industrial automation and aerospace & defense. The IPC1710 is application-agnostic, cost effective, standard compliant IEEE 1588 v2 Slave/Master, supporting G.8261, G.8265.1, G.8275.1 and G.8275.2. The IPC1710 is designed for easy field upgrades to support future enhancements as well as future synchronization standards.
The IPC1710 is a chip on FPGA leveraging Xilinx® Spartan™ 6 FPGA supporting 16MB of FLASH memory and 64MB of DDR II memory.

IPC1710 Functional Block Diagram



The IPC1710 can be set to operate as either IEEE 1588 master or slave. The IEEE 1588 protocol is a bidirectional protocol requiring all ports to transmit and receive IEEE 1588 packets. Each packet received its time-stamp by the Timestamp Generator and classified by the Classifier. In the case the packet is IEEE 1588 packet it is sent to the Pre-Processor along with its timestamp. The Pre-Processor is transferring the received general packets to the PTP Manager and Stack for further processing. In the case of IEEE 1588 event packet the Pre-Processor compensate for part of the packet network impairments and prepare the data for the Sync Processor. The Sync Processor is comprised of a suite of algorithms that processes the data and controls the 1PPS PLL, the programmable clock output of the Clock Generator, and the ToD. The ToD is communicating with the ToD UART utilizing the NMEA protocol for either providing or getting the ToD from a GPS. The IEEE 1588 packets are transmitted by the Packet Generator which is controlled by the PTP Manager and Stack. Each packet transmitted is time-stamped by the Timestamp Generator and this timestamp is either embedded into the packet or sent to the Pre-Processor depending on the packet type and selected mode of operation.

Main Features and Benefits

- Standalone IEEE 1588 v2 standard compliant Master/Slave chip on FPGA
- Excellent synchronization performance over most extreme packet transport network conditions
- Slave meets 3G, 4G-LTE and 5G synchronization requirements
- Adaptive to network impairments
- Typical lock time better than 10 sec
- Slave ToD phase error is better than ±1µsec, and frequency accuracy is better than 16ppb, on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- Hybrid IEEE 1588/SyncE support. Requires external SyncE PLL
- Supported IEEE 1588 profiles: G.8265.1, G.8275.1 and G.8275.2
- Supports up to 64 slaves/channels
- Supports Unicast/Multicast
- Supports one step / two steps
- Low total cost of ownership
- Zero touch approach can make external CPU redundant
- Upgradeable by software
- Easy adding of enhancements and supporting emerging clock synchronization standards
- Operates with either TCXO or OCXO (10MHz, 12.8MHz or 20MHz)
- Interfacing generic PHY
- Modes of operation: Free run, Trace, Lock and Holdover
- Utilize Xilinx's Spartan 6 FPGA - XC6SLX45
- 324 pin BGA, 15 mm x 15 mm,0.8 mm pitch RoHS package

(*) The performance tested under the ITU-T G.8261 tests suite provide an indication for IPClock's technology capabilities and is not guaranteed across all types of network elements and networks conditions. Please contact IPClock's support for more information.