IPCLOCK

IPC9010

IEEE 1588 Boundary, Slave and Master Clocks
IP Core
DATASHEET

About the IPC9010

The IPC9010 utilizes IPClock's state-of-the-art IEEE 1588 v2 technology optimized for providing high quality frequency synchronization and Time of Day (ToD) over packet transport networks. Clock synchronization is required by many wireline and wireless applications including 3G, 4G-LTE, 5G, Smart Grid, Industrial automation and aerospace and defense. The IPC9010 is application-agnostic, cost effective, standard compliant IEEE 1588 v2 BC/Slave/Master, supporting G.8261, G.8265.1, G.8275.1 and G.8275.2. The IPC9010 is designed for easy field upgrades to support future enhancements as well as future synchronization standards.

The IPC9010 is a IP core leveraging Xilinx® Zynq FPGA requires 16MB of QSPI FLASH memory and 128MB of DDR3 memory.

Main Features and Benefits

- Standalone IEEE 1588 v2 standard compliant boundary, slave and master clocks IP core
- Excellent synchronization performance over most extreme packet transport network conditions
- Slave meets 3G, 4G-LTE and 5G synchronization requirements
- Adaptive to network impairments
- Typical lock time better than 10 sec
- Slave ToD phase error is better than ±1µsec, and frequency accuracy is better than 16ppb, on a managed 10-switch GbE network under ITU-T G.8261 conditions (*)
- GMII interface
- Hybrid IEEE 1588/SyncE support. Requires external SyncE PLL.
- Supports APTS (Assisted Partial Timing Support)
- Supported IEEE 1588 profiles: G.8265.1, G.8275.1 and G.8275.2
- Supports up to 64 slaves/channels
- Supports Unicast/Multicast
- Supports one step / two steps
- Low total cost of ownership
- Zero touch approach can make external CPU redundant
- Easily integrates in existing and next generation designs
- Upgradeable by software
- Easy adding of enhancements and supporting emerging clock synchronization standards
- Interfacing generic PHY
- Master can lock to undisciplined 1PPS signal from GPS
- Standard compliant Best Master Clock (BMC) algorithm
- Modes of operation: Free run, Trace, Lock and Holdover
- Flexible reference clock input: 1PPS, 1.544MHz, 2.048MHz, or 10MHz
- Programmable clock output frequencies: 1.544MHz, 2.048MHz, or 10MHz
- Utilize Xilinx's Zynq FPGA

(*) *The performance tested under the ITU-T G.8261 test suite provide an indication for IPClock's technology capabilities and is not guaranteed across all types of network elements and network conditions. Please contact IPClock's support for more information.*

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1 Reference System Diagram

Figure 1 below depicts common network architecture including frequency and/or time of day (ToD) distribution over packet transport network using IEEE 1588 boundary clock (BC), and ordinary clock (OC) that may be integrated in each network element and in the Grandmaster.

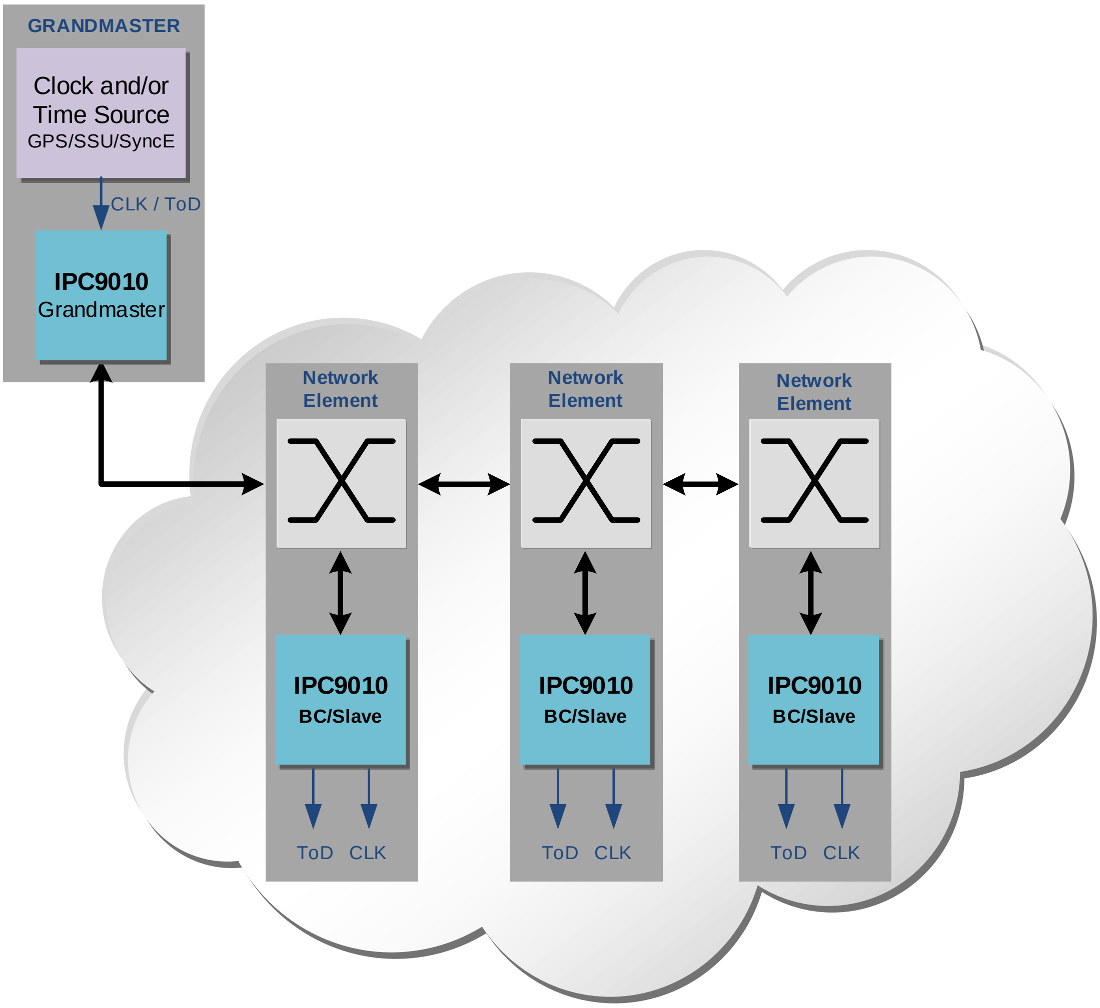

Figure 1: Accurate Time of Day, 1PPS and Frequency Distribution

The Grandmaster incorporates the IPC9010 in order to lock to a reference clock contains either 1PPS and ToD from a GPS receiver, or other clocks from other sources such as SSU. Each network element includes the IPC9010 uses for clock recovery, implementing IEEE 1588 standard compliant boundary clock (BC) or Slave.

The IPC9010 is not in-line with the data path. Instead, the IPC9010 connects to a switch or network processor (NP) that separates the PTP packets from the user data and directs the PTP traffic to/from the IPC9010.

2 General Description

The IPC9010 is an IEEE 1588 standard compliant standalone boundary clock (BC), Slave or Master core. The mode of operation (BC/Slave/Master) can be changed using the IPC9010 application-programming interface (API) functions. When set to work in BC and Slave mode, the IPC9010 is synchronizing its real time clock to the Master's real time clock. Powered by IPClock's state-of-the-art clock synchronization algorithms suite, the IPC9010 is capable of achieving cutting edge synchronization performance. IPClock's algorithm suite is capable of filtering out the impacts of the packet transport network impairments on IEEE 1588 packets, which results packet delay variation, packet loss, packet duplication, and network re-route.

When set to work in BC/Master modes, the IPC9010 supports up to 64 Slaves. The IPC9010 supports unicast and multicast operation.

Both Master and Slave have precision holdover allowing maintaining adequate clock synchronization in case reference clock signal is not available or degraded. In holdover, the clock synchronization performance dependents on the oscillator quality. Proper oscillator should be selected to meet the application's time-of-day and frequency accuracy requirements. The IPC9010 is supporting a variety of IPClock approved oscillators.

The IPC9010 includes all the functionality required for implementing a complete standalone IEEE 1588 BC/Slave/Master core including hardware assist functionality, clock synchronization algorithms suit (also known as servo) and standard compliant IEEE 1588 protocol stack. The IPC9010 can operate with any 3rd party SyncE PLL in order to enable formation of high performance hybrid IEEE 1588 and SyncE.

The IPC9010 is an IP core for Xilinx's Zynq FPGAs, provides application-agnostic, cost effective, reliable and standard compliant solution that can easily integrate into existing and next generation designs. Being an IP core the IPC9010 can be simply upgraded by downloading new configuration and/or software files allowing easy addition of enhancements as well as updates required for supporting emerging clock synchronization standards.
By default, the IPC9010 start operates as IEEE 1588 BC. Default configuration values can be modified using the IPC9010 application-programming interface (API) package for configuring as well as for controlling and monitoring the IPC9010. The APIs allow software developers to easily configure, control and monitor the IPC9010.

3 Functional Block Diagram

The IPC9010 functional block diagram is given in Figure 2 below.

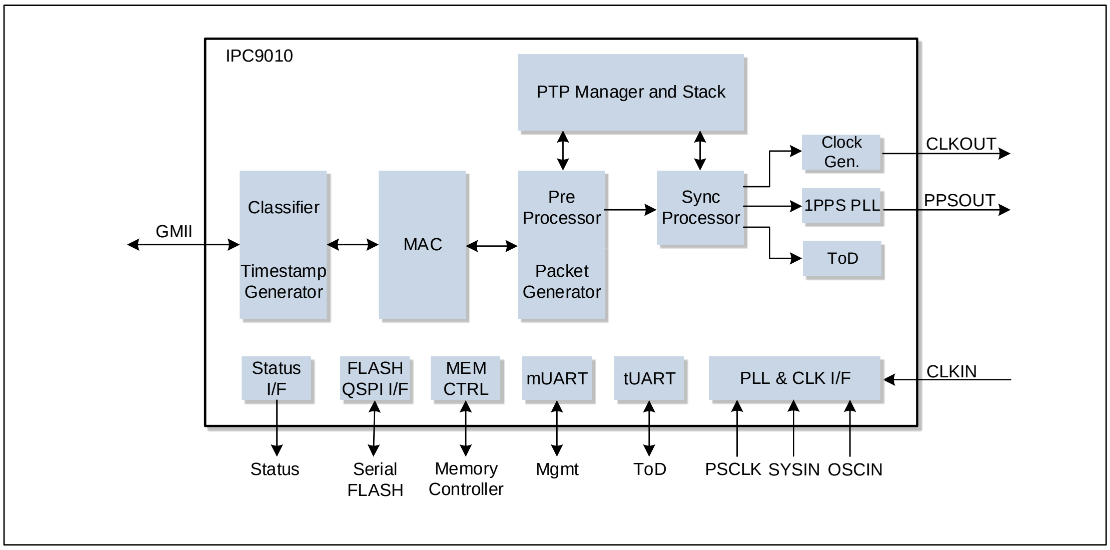

Figure 2: IPC9010 Functional Block Diagram

The IPC9010 can be set to operate as either IEEE 1588 BC or Slave or Master clock. The packets are been classified by the Classifier and get time-stamped by the Timestamp-Generator. In the case the packet is IEEE 1588 packet it is sent to the Pre-Processor along with its timestamp. The Pre-Processor is transfers the received general PTP packets to the PTP Manager and Stack for further processing. In the case of IEEE 1588 event packet the Pre-Processor compensate for part of the packet network impairments and prepares the data for the Sync-Processor. The Sync-Processor is comprised of a suite of algorithms that process the data and controls the ToD, 1PPS, and Clock-Generator modules. The ToD module communicates with the tUART (ToD UART) utilizing the NMEA protocol for either providing or getting the ToD from a GPS. The IEEE 1588 packets are transmitted by the Packet-Generator which is controlled by the PTP Manager and Stack. The mUART module is the management UART used by host CPU for locally configure, control, and monitor the core either by external CPU or using local terminal. The Status I/F provides the core status. The FLASH QSPI I/F module is a standard quad serial port interface for interfacing with the QSPI FLASH. The FLASH is used for loading the core software and storing the core configuration. The DDR Controller module is the interface for the DDR3 memory.

The IPC9010 supports wide variety of operation modes such as IEEE 1588 BC, Slave, Master, Hybrid BC and Hybrid Slave. The PLL & CLK I/F module supports those modes and generates all the clocks require for the IPC9010 operation. The IPC9010 can be fed by three system clocks. The OSCIN, SYSIN and PSCLK. The OSCIN shall be driven from IPClock's approved local oscillator or from high quality external PLL. In case of using oscillator, the minimal requirements are: free-run accuracy 4.6ppm, frequency stability over temperature range up to 50ppb, frequency slop up to 2ppb/'C. The SYSIN can be driven by SyncE PLL. The PSCLK shall be driven by PS PLL. The PSCLK shall be fed by 33.33MHz XO for CPU operation.

The IPC9010 has GMII interface for interfacing with Ethernet SGMII GTX or to generic Ethernet PHY. It requires 128MB of DDR3 memory and 16MB QSPI FLASH memory.

4 IPC9010 Package Description

Table 1 presents the IPC9010 Package.

File Name	Description
ipc9010.dcp	IPC9010 netlist
ipc9010.v	IPC9010 top
ipc9010.xdc	IPC9010 constrains
IPC.elf.gz	IPC9010 application

Table 1: IPC9010 Package Description

For detailed package description, as well as FPGA bit file generation, refer to the integration guide.

5 Reference Design

Figure 3 presents IPC9010 reference design on Xilinx® ZC706 EVB Rev 2.0. In order to instantiate the IPC9010 into a design, FPGA adaptation layer need to be added by the user. An example for the adaptation layer targeted to operate the IPC9010 on Xilinx® ZC706 EVB is delivered in addition to the IPC9010. The reference design includes 1G SFP Ethernet 1000base-T interface. The core access 32-bit DDR3 Memory using 1066MHz speed. As an option, Xilinx® FMC XM105 can be mounted on ZC706 EVB at FMC-LPC socket in order to have additional clock options.

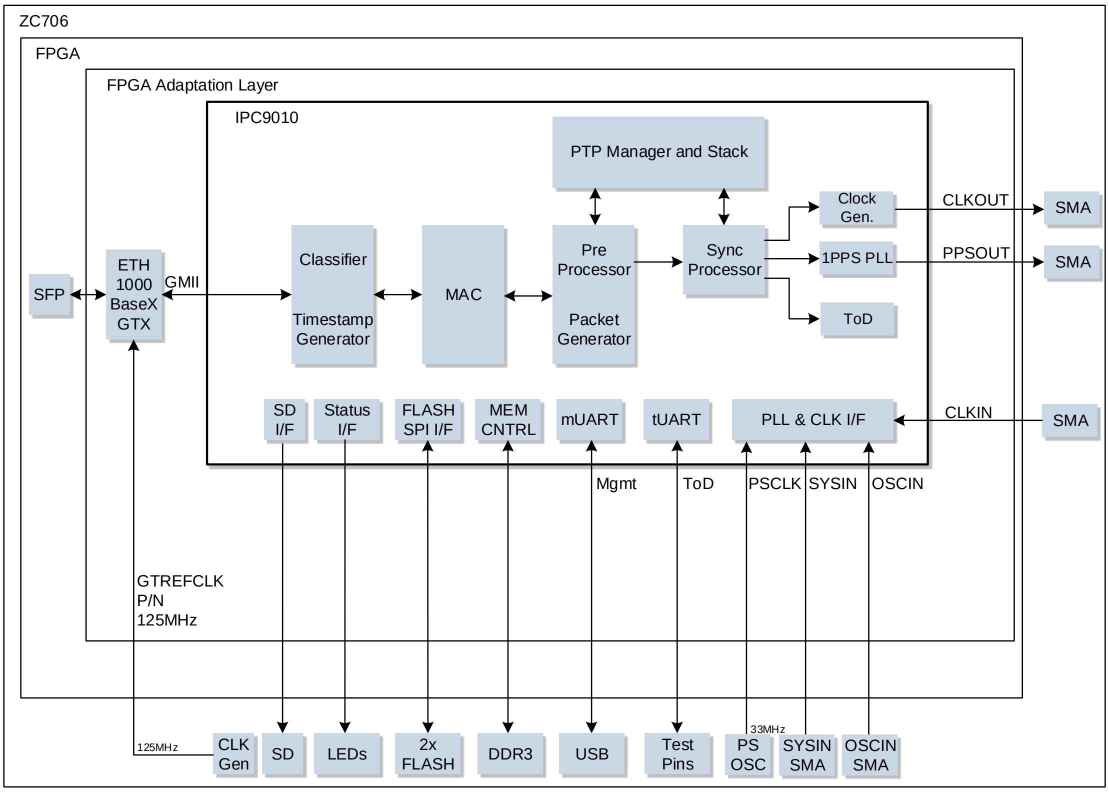

Figure 3: IPC9010 Reference Design on Xilinx® ZC706

Table 2 presents the LEDs assignment using 4-pin GPIO_LEDS. The LEDs are marked as item 22 in Figure 4.

LED #	LED Silk	Signal	Description
DS8	L	STATFR	PTP free run status output (off-not FR, on-FR)
N/A	-	STATTR	PTP trace status output (off-not TR, on-TR)
DS9	C	STATHO	PTP holdover status output (off-not HO, on-HO)
DS10	R	STATLK	PTP lock status output (off-not LK/TR, blink-TR, on-LK)
N/A	-	STAT[0]	General status output bit 0
DS35	0	STAT[1]	General status output bit 1 (off-FAIL, blink-ALARM, on-PASS)

Table 2: ZC706 LEDs Description

Table 3 presents the LEDs assignment using FMC 4-pin GPIO_LEDS. The LEDs are marked as item 8 in Figure 5.

LED #	LED Silk	Signal	Description
DS1	DS1	STATFR	PTP free run status output (off-not FR, on-FR)
N/A	-	STATTR	PTP trace status output (off-not TR, on-TR)
DS2	DS2	STATHO	PTP holdover status output (off-not HO, on-HO)
DS3	DS3	STATLK	PTP lock status output (off-not LK/TR, blink-TR, on-LK)
N/A	-	STAT[0]	General status output bit 0
DS4	DS4	STAT[1]	General status output bit 1 (off-FAIL, blink-ALARM, on-PASS)

Table 3: FMC LEDs Description

Table 4 presents the SMAs utilization.

SMA #	Signal	Description
J67	OSCIN	20MHz Oscillator In (2.5v). Marked as item 9 in Figure 4

SMA #	Signal	Description
J68	PPSOUT_SYSIN_CLKIN	Option-1: FMC not mounted. PPSOUT or SYSIN or CLKIN (2.5v). Marked as item 9 in Figure 4 Option-2: FMC mounted. CLKIN (2.5v). Marked as item 9 in Figure 4 PPSOUT shall be configured as three state using API

Table 4: SMAs Description

Table 5 presents the SMAs – FMC utilization (optional).

SMA #	Signal	Description
J9	CLKOUT_SYSIN	CLKOUT or SYSIN (2.5v). Marked as item 14 in Figure 4
J10	PPSOUT	One pulse per second output (2.5v). Marked as item 14 in Figure 4

Table 5: SMAs Description – FMC

Table 6 presents the CLKIN / SYSIN and FMC control using SW12 DIP Switch. The switch is marked as item 24 in Figure 4.

SW12 pin#	Mode	Description
1	0 - CLKIN	CLKIN/SYSIN input selector for J68 SMA
	1 - SYSIN	
2	0 - Off	LPC FMC XM105 connected (optional)
	1 - On	
3	N/A	N/A
4	N/A	N/A

Table 6: SW12 DIP Switch Control

Table 7 presents the clock signal configuration.

#	PTP Config	Boards	SW12				API	OSCIN	SYSIN	CLKIN	PPSOUT	CLKOUT
			1	2	3	4						
1	M	ZC706	0	0	X	X	See 3a	J67 SMA	N/A	J68 SMA	J58.7	J58.1
2	S/BC	ZC706	X	X	X	X	See 3b	J67 SMA	N/A	J58.2	J68 SMA J58.7	J58.1
3	M/S/BC +SYSIN	ZC706	1	0	X	X	See 3a	J67 SMA	J68 SMA	J58.2	J58.7	J58.1
4	M/S/BC +SYSIN	ZC706 +FMC	1	1	X	X	See 3a	J67 SMA	J68 SMA	J9 SMA(F)	J10 SMA(F) J58.7 J1.2(F)	J58.1 J1.39(F)

Table 7: Clock Signals Configuration

Comments:
1. All PTP configurations above support Master, Slave and BC configurations. However due to limited SMA connectors, one can select the optimal PTP configuration in terms of SMA usage.
2. PTP Config – M: Master, S: Slave, BC: Boundary Clock
3. API
   (a) - using SetPpsOutMode(0,5) API for setting PPSOUT to three-state
   (b) - using SetPpsOutMode(0,1) API for clearing PPSOUT three-state
4. The (F) marked FMC
5. X – Do not care

Figure 4 presents the Xilinx® ZC706. Description of ZC706 is available at Xilinx's UG954 - ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide.

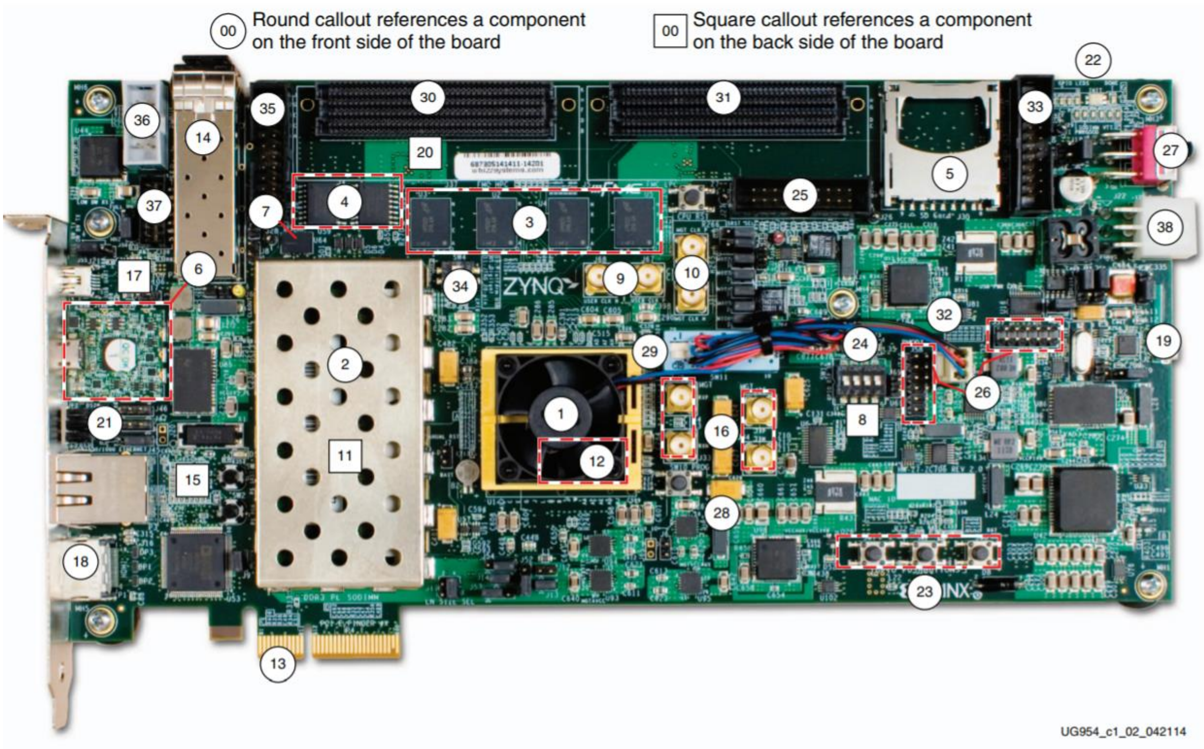

Figure 4: Xilinx® ZC706 EVB

Comments:

- The reference design was verified using 1000Base-T SFP of LinkTel LX1801INL connected to item 14 in Figure 4.
- The mUART is been connected to the Mini-B USB connector marked as item 21 in Figure 4.

Due to ZC706 hardware limitations the following are not available on the demo platform:

1. ToD via UART port. However, ToD can be set or get using APIs, and ToD signals (TUTX, TURX) are available on J58.6 J58.8 pins respectively. The J58 is marked as item 26 in Figure 4.
2. IPClock's approved oscillator for high quality PTP operation. However high quality external clock can be provided by the user via SMA J67. In case high quality is not no available via J67, the PSCLK is been used by the IPC9010.

Figure 5 presents the optional Xilinx® FMC XM105. Description of XM105 is available at Xilinx's - UG 537 FMC XM105 Debug Card User Guide.

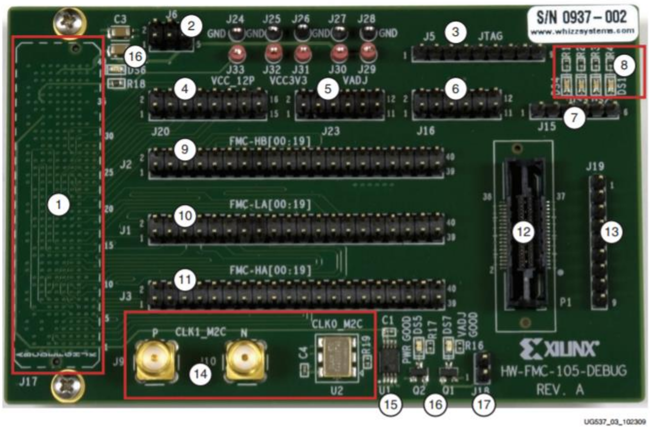

Figure 5: Xilinx® FMC XM105

6 Resources

6.1 IPC9010

Table 8 presents the IPC9010 FPGA netlist resources.

Resources Type	Resources
Register	6400
LUT	7700
BRAM	3
DSP	22
GTX	0
MMCM	1
PLL	2
BUFGCTRL	11

Table 8: IPC9010 FPGA resources

NOTE: The user shall have additional margin of about 15% of the Register, LUT, BRAM, DSP and BUFGCTRL for future upgrades.

6.2 IPC9010 with adaptation layer on ZC706

Table 9 presents the IPC9010 FPGA resources with adaptation layer on ZC706. The resources includes Gig_ethernet_pcs_pma core.

Resources Type	Resources
Slice	3000
Register	7400
LUT	8000
BRAM	3
DSP	22
GTX	1
MMCM	2
PLL	2
BUFGCTRL	20

Table 9: IPC9010 FPGA resources with adaptation layer on ZC706

7 Operational Description

The IPC9010 is providing applications with precision clock and time of day (ToD) synchronization over packet transport networks. The IPC9010 can be set to operate as either IEEE 1588 boundary clock (BC), slave or master.

The IEEE 1588 protocol is a bidirectional protocol requiring the BC, slave and master to transmit and receive IEEE 1588 packets. The packets exchange is used by the BC slave port or by the slave to calculate the delay to the selected master in order to align its real time clock to the master's real time clock. The calculations are based on measuring the roundtrip delay between the slave and the master. The measured roundtrip is divided by two to get the trip delay from the master to the slave.

The delay measurement calculations defined in the IEEE 1588 standard assume that networks are symmetrical. Any asymmetry between the path of the sync packets and the path of the delay request packets will cause an inherent offset to the slave's real time clock relative to the master's real time clock. There are many reasons for network asymmetries. Some of the network asymmetries can be compensated by implementing BC or transparent clock (TC) or a combination of both in the network. For example, the IPC9010 can be added to network elements to compensate for network asymmetry. In addition, adding BC functionality to network elements will reduce the amount of packet delay variation which will allow the IEEE 1588 slaves to improve their synchronization performance.

7.1 Administrative State Machine

The IPC9010 administrative state diagram is shown in Figure 6 below.

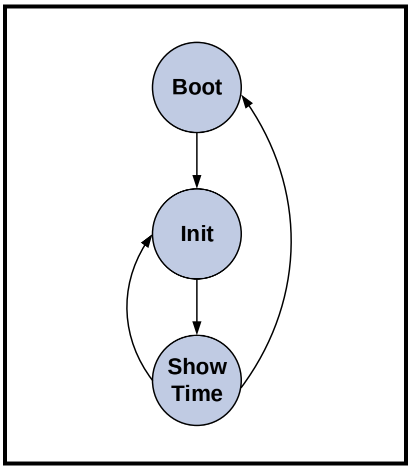

Figure 6: IPC9010 Administrative State Machine

After downloading the code into the IPC9010, it will enter the Boot state. In this state, the IPC9010 is performing sanity tests like code integrity. The IPC9010 will continue to the Init state upon successful completion of the tests in the Boot state. In the Init state, the IPC9010 is preparing for operation by initializing the hardware, protocol stack and servo. It configures the core for the proper mode of operation according to the configuration parameters stored in FLASH memory or as default. After initialization, the IPC9010 will perform comprehensive Init BIST (Built in Self-Test). Upon successful completion of the Init BIST, the IPC9010 will transition to Showtime state. In Showtime state, the IPC9010 invokes the IEEE 1588 stack and servo. By default, the IPC9010 is set to BC mode of operation. While in Showtime state, Showtime BIST is been performed. Hardware reset return the core to Boot state. By using Reset / Stop / Start APIs the core returns to Init state. See the user guide for more details regarding the core BIST, Reset, Stop and Start.

The STATFR, STATHO, STATTR, STATLK, and STAT[1:0] signals are indicating the core status. While IPC9010 is in Boot or Init state, all signals are 0 (low). While IPC9010 is in Showtime state, the signals are been controlled by the core state machine as describes in the following chapters.

7.2 Core State Machine

7.2.1 BC and Slave Modes

Figure 7 below depicts the IPC9010 core state-machine when in BC or slave modes.

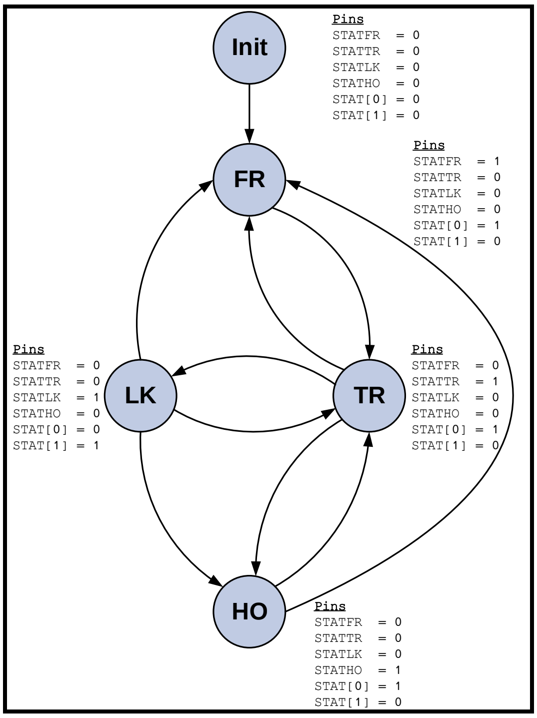

Figure 7: Core State-Machine – Slave and BC Modes

The core starts in Init state. In this state, the core is preparing for operating. Once completed, the core will transition to free run (FR) state. The core will transition to trace (TR) state when a valid IEEE 1588 packet stream is detected by the slave port.

In TR state, the core is waiting for the slave port to attempt locking to the master. If successful, the core will transition to lock (LK) state. In case the core will be unable to lock to the master within 120 minutes, it will transition to free run (FR) state.

In case the slave port lost the IEEE 1588 packet stream from its master, and the core is not in holdover ready state, the core will transition to free run (FR) either from LK state or from TR state. In case the core is in holdover ready state, the core will transition to holdover (HO) either from LK state or from TR state. The core will transition from HO to FR state in case the slave port was in HO state for a consecutive hoSpecModeExTh sec while in hoSpecModeEx=1. The core will transition to TR state should the packet stream resumes to the slave port.

Valid IEEE 1588 packet stream is defined using the Communication path (Commpath) term. The Commpath, is the PTP Sync/FU and DelayResp packets path between a master port and a slave port. The slave Commpath state (slaveCommpathState) indicates the current Commpath as been monitored by the slave port.

Up Commpath state (slaveCommpathState=1) indicates that the slave is receiving both Sync/FU packets and DelayResp packets, as expected. The transition to up Commpath state is pending detection of sequential series of 15 Sync/FU packets followed by one sec duration with one delay response packet or more.

Down Commpath state (slaveCommpathState=0) indicates that the slave is neither receiving Sync packets nor DelayResp Packets. The Commpath is down in case:

- No Sync packets for more than 1 sec
- No DelayResp packets for more than 30 sec.

STATFR, STATTR, STATLK, STATHO and STAT[1:0] Signals are indicating the core state and status. See the user guide for more details regarding the core states.
The table below summarizes the state transitions events.

Transition	Event
➔ Init	Power up.
Init ➔ FR	Initialization completed and BIST pass.
FR ➔ TR	***slaveCommpathState=1*** as reported by ***GetCommpathState***.
TR ➔ LK	***slaveCommpathState=1*** as reported by ***GetCommpathState*** and estimated phase error is within the defined threshold. The estimated phase error presented by ***slaveStateEx*** as reported by ***GetState*** API. The transition is determined by ***slaveStateEx*** and by ***slaveStateLkTh***, set by ***SetStateSlaveLkTh*** API.
TR ➔ HO	***slaveCommpathState=0*** as reported by ***GetCommpathState***, while ***slaveStateHoReady*** as reported by ***GetHoRdy*** is greater than 0.
LK ➔ TR	***slaveCommpathState=1*** as reported by ***GetCommpathState***, and estimated phase error is exceeding the defined threshold. The estimated phase error presented by ***slaveStateEx*** as reported by ***GetState*** API. The transition is determined by ***slaveStateEx*** and by ***slaveStateLkTh***, set by ***SetStateSlaveLkTh*** API.
LK ➔ HO	***slaveCommpathState=0*** as reported by ***GetCommpathState***, while ***slaveStateHoReady*** as reported by ***GetHoRdy*** is greater than 0.
LK ➔ FR	***slaveCommpathState=0*** as reported by ***GetCommpathState***, while ***slaveStateHoReady*** as reported by ***GetHoRdy*** is 0.
HO ➔ TR	***slaveCommpathState=1*** as reported by ***GetCommpathState***.
HO ➔ FR	Consecutive ***hoSpecModeExTh*** sec in HO state while in ***hoSpecModeEx=1*** as set by ***SetHoSpecModeEx*** API
TR ➔ FR	***slaveCommpathState=0*** as reported by ***GetCommpathState***, while ***slaveStateHoReady*** as reported by ***GetHoRdy*** is 0, or in TR state for more than consecutive ***hoSpecModeExTh*** sec while ***hoSpecModeEx=1*** as set by ***SetHoSpecModeEx*** API.

Table 10: Core State Transition Events Table – Slave and BC Modes

7.2.2 Master

Figure 8 below depicts the core state-machine when in master mode.

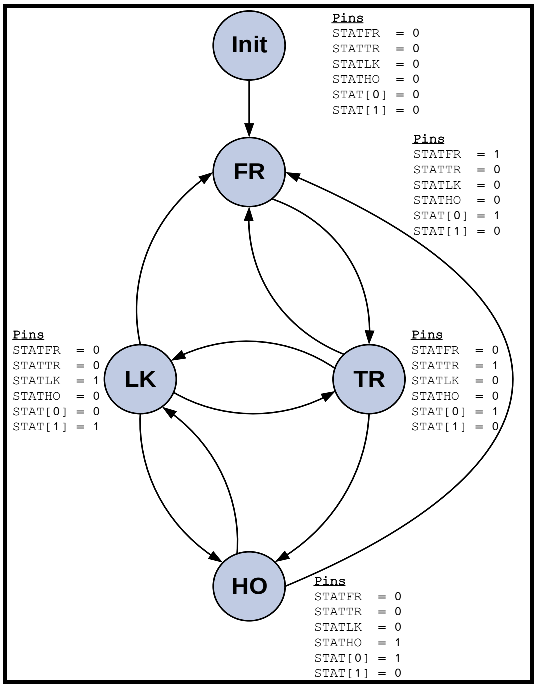

Figure 8: Core State-Machine – Master Mode

The core starts in Init state. In this state, the core is preparing for operating. Once completed, the core will transition to free run (FR) state. The core will transition to trace (TR) state when a 1PPS signal or reference clock is detected (according to configuration).

In TR state, the core is waiting for the master port to attempt locking to the 1PPS signal or reference clock. If successful, the core will transition to lock (LK) state. In case the core will be unable to lock within clkInPllRlkTh minutes, it will transition to free run (FR) state.

In case the master port lost its 1PPS signal or reference clock, and the core was never been in LK state, the core will transition to free run (FR) either from LK state or from TR state. In case the core was in LK state, the core will transition to holdover (HO) either from LK state or from TR state. The core will transition from HO to FR state in case the master port was in HO state for a consecutive clkInPllRlkTh minutes. In case core in HO, and 1PPS signal or reference clock resumed and it is aligned with the core internal clock, the core will transition from HO to LK. In case of 1PPS signal or reference clock resumed and is not aligned with the core internal clock, the core will transition from HO to FR then TR, and in case lock conditions met, will transition to LK.

STATFR, STATTR, STATLK, STATHO and STAT[1:0] signals are indicating the core state and status. See the core user guide for more details regarding the core states.

The table below summarizes the state transitions events.

Transition	Event
➔ Init	Power up
Init ➔ FR	Initialization completed and BIST pass.
FR ➔ TR	1PPS signal or reference detected
TR ➔ LK	Estimated phase synchronization error estimated ≤100ns
TR ➔ HO	1PPS signal or reference clock is lost
LK ➔ TR	Estimated phase synchronization error estimated ≤100ns
LK ➔ HO	1PPS signal or reference clock is lost
HO ➔ LK	1PPS signal or reference clock resumed and estimated phase synchronization error estimated ≤100ns
HO ➔ FR	Consecutive ***clkInPllRlkTh*** minutes, as set by ***SetClkInPllRlkT***h API, in HO state or 1PPS signal or reference clock resumed and is not aligned with the device internal clock
TR ➔ FR	Consecutive ***clkInPllRlkTh*** minutes, as set by ***SetClkInPllRlkT***h API, in TR state

Table 11: Core State Transition Events Table – Master Mode

8 Interface Signals Description

This section provides information describing the signals in the IPC9010. The signals description is organized in tables. Each table provides information for specific interface or signals group. The following convention is used:

Signal	I/O	Description
Signal Symbol	I – Input O – Output I/O – Input/Output	Short description

Table 12 below defines the IPC9010 reset signals.

Symbol	I/O	Description
PSPORn	I	Active-low power on reset
PSSRSTn	I	Active-low system reset
PL_RESETn	O	Active-low PL reset signal from the PS, activated when PSPORn or PSSRSTn become active and it remains active until the PS is out of its boot sequence. It is used to reset the PL logic.

Table 12: Reset Signal Description

Table 13 below defines the IPC9010 GMII Ethernet interface signals.

Signal	I/O	Description
GMII_TX_CLK	I	GMII transmit clock to Ethernet GTX or to PHY
GMII_TX_EN	O	GMII transmit data enable control to Ethernet GTX or to PHY
GMII_TX_ER	O	GMII transmit error control to Ethernet GTX or to PHY
GMII_TXD[7:0]	O	GMII transmit data bus to Ethernet GTX or to PHY (7 is MSbit)
GMII_RX_CLK	I	GMII receive clock from Ethernet GTX or from PHY
GMII_RX_DV	I	GMII receive data valid control from Ethernet GTX or from PHY
GMII_RX_ER	I	GMII receive error control from Ethernet GTX or from PHY
GMII_RXD[7:0]	I	GMII receive data bus from Ethernet GTX or from PHY (7 is MSbit)
GMII_MDC	O	GMII management data clock
GMII_MDIO_I	I	GMII management data Input
GMII_MDIO_O	O	GMII management data output
GMII_MDIO_T	O	GMII management data output Three-state

Table 13: GMII Ethernet Interface Signal Description

Table 14 below defines the IPC9010 DDR memory interface signals.

Symbol	I/O	Description
DDRDQ[31:0]	I/O	DDR 23 bit data bus
DDRBA[2:0]	O	DDR 3-bit bank address bus
DDRA[14:0]	O	DDR 15-bit address bus
DDRDQSP[3:0]	I/O	DDR 4-bit data strobe positive bus, 1-bit per byte for DDRDQ[31:0]
DDRDQSN[3:0]	I/O	DDR 4-bit data strobe negative bus, 1-bit per byte for DDRDQ[31:0]
DDRDM[3:0]	O	DDR 4-bit data mask bus, 1-bit per byte for DDRDQ[31:0]
DDRRASn	O	DDR active-low row address strobe
DDRCASn	O	DDR active-low column address strobe
DDRWEn	O	DDR active-low write enable
DDRODT	O	DDR on-die termination control
DDRRESETn	O	DDR active-low reset
DDRVRP	I	DDR DCI voltage reference positive
DDRVRN	I	DDR DCI voltage reference negative
DDRCSn	O	DDR active-low chip select
DDRCLKP	O	DDR clock positive
DDRCLKN	O	DDR clock negative
DDRCLKE	O	DDR clock enable

Table 14: DDR Memory Interface Signal Description

Table 15 below defines the IPC9010 dual QSPI FLASH memory interface signals.

Symbol	I/O	Description
QSPI0_IO[3:0]	I/O	QSPI0 4-bit data bus
QSPI0SSn	O	QSPI0 Master Chip Select Output. Active Low. Connect to the QSPI0 FLASH Slave Select input.
QSPI0_CLK	O	QSPI0 Configuration clock. Connect to the QSPI0 FLASH clock input.
QSPI1_IO[3:0]	I/O	QSPI1 4-bit data bus
QSPI1SSn	O	QSPI1 Master Chip Select Output. Active Low. Connect to the QSPI1 FLASH Slave Select input.
QSPI1_CLK	O	QSPI1 configuration clock. Connect to the QSPI1 FLASH clock input.
QSPI_FBCLK	O	QSPI feedback clock

Table 15: SPI FLASH Interface Signal Description

Table 16 below defines the IPC9010 clock interface signals.

Symbol	I/O	Description
OSCIN	I	20MHz – Oscillator input for PTP
PSCLK	I	33.33MHz PS clock input.
SYSIN	I	125MHz system clock input for interfacing with SyncE PLL
CLKIN	I	Reference clock input
PPSOUT_C	O	One pulse per second output clock
PPSOUT_T	O	One pulse per second output three-state
CLKOUT_C	O	Clock output clock
CLKOUT_T	O	Clock output three-state
CLKA	O	One pulse per second output for interfacing with other devices (e.g. PLL, PTP PHY)
CLKB	O	One pulse per second output for interfacing with other devices (e.g. PLL, PTP PHY)
FCLK_100M	O	PS 100MHz clock base on PSCLK
FCLK_125M	O	PS 125MHz clock base on PSCLK
FCLK_25M	O	PS 25MHz clock base on PSCLK
FCLK_200M	O	PS 200MHz clock base on PSCLK

Table 16: Clock Interface Signal Description

Table 17 below defines the IPC9010 reserved clock interface signals.

Symbol	I/O	Description
SYSINA	I	Reserved
CLKINS	I	Reserved
ETHRXCLKI1	I	Reserved
ETHRXCLKO1	O	Reserved
PTPREFCLK	O	Reserved
ETHREFCLK	O	Reserved
ETHCLKIN	I	Reserved
CLKC	I	Reserved
CLKD	I	Reserved
CLKF	I	Reserved

Table 17: Reserved Clock Interface Signal Description

Table 18 below defines the IPC9010 management UART (mUART) interface signals.

Symbol	I/O	Description
MUTX	O	Management UART transmit signal
MURX	I	Management UART receive signal

Table 18: Management UART (mUART) Interface Signal Description

Table 19 below defines the IPC9010 ToD UART (tUART) interface signals.

Symbol	I/O	Description
TUTX	O	ToD UART transmit signal
TURX	I	ToD UART receive signal

Table 19: ToD UART (tUART) Interface Signal Description

Table 20 below defines the IPC9010 status interface signals.

Symbol	I/O	Description
STATFR	O	Free run status output
STATTR	O	Trace status output
STATLK	O	Lock status output
STATHO	O	Holdover status output

Symbol	I/O	Description
STAT[1:0]	O	General status output 2-bit data bus (for 2-color LEDs). For 1-color LED use only STAT[1].

Table 20: Status Interface Signal Description

Table 21 below defines the IPC9650 SDIO interface signals.

Symbol	I/O	Description
SD0_CLK	I/O	SD0 card clock
SD0_CMD	I/O	SD0 card command
SD0_DATA[3:0]	I/O	SD0 card 4-bit data bus
SD0_CD	I	SD0 card detect
SD0_WP	I	SD0 card write protect

Table 21: SDIO Signal Description

Table 22 below defines the IPC9010 I2C interface signals. The I2C interface shall be used only for the reference design on ZC706.

Symbol	I/O	Description
I2C0_SCL	O	I2C0 clock
I2C0_SDA	I/O	I2C0 data
I2C0_RSTn	I/O	Active-low I2C0 reset

Table 22: I2C Signal Description

9 Interfaces Description

9.1 Reset

The IPC9010 has 2 resets input signals: PSPORn and PSSRSTn. The core will be set to Boot administrative state when asserting the PSPORn / PSSRSTn signal. For detail information on the administrative state see Administrative State Machine chapter.

PSPORn – Power-on reset: The power-on reset is the master reset of the entire chip and IPC9010 core. It also reset the PS clock generator.

PSSRSTn – System reset: The system reset allows to reset the entire chip and this core. It does not reset the PS clock generator.

For detail explanation on the PSPORn and PSSRSTn reset sequence see Xilinx AC & DC switching characteristic document (DS187) and Zynq-7000 All Programmable SoC Technical Reference Manual (UG585).

The IPC9010 has reset output signal PL_RESETn which can be used for PL reset. It is an active-low PL reset signal from the PS, activated when PSPORn or PSSRSTn become active and it remains active until the PS is out of its boot sequence.

9.2 Ethernet GMII Interface

The GMII interface (ETH1) shall be connected to Ethernet GTX or to generic Ethernet PHY.

9.3 DDR Memory Interface

The IPC9010 requires 32-bit DDR3 memory device with at least 128MB with speed of 1066MHz. For detailed design and layout consideration using DDR3 please look at Xilinx PCB design guide (PG933).

9.4 QSPI FLASH Memory Interface

The IPC9010 requires double 16MB QSPI memory devices. The dedicated QSPI FLASH memories is used for faster uploading the IPC9010 software as well as for storing/recalling the IPC9010 configuration database.

9.5 PLL & CLK Interface

The IPC9010 supports wide variety of operation modes such as IEEE 1588 BC, Master, Slave, Hybrid and APTS. The PLL & CLK I/F module supports those modes and generates all the clocks require for the IPC9010 operation.

9.5.1 OSCIN

The OSCIN is a 20MHz clock, typically generated by IPClock's approved local oscillator or by high quality external PLL (e.g. SyncE PLL). The OSCIN is mandatory for high quality PTP operation, however for native evaluation purposes, it maybe optional. The OSCIN minimal requirements are: free-run accuracy 4.6ppm, frequency stability over temperature range up to 50ppb, frequency slop up to 2ppb/'C. In case of unstable clock, the entire clock recovery may be severely damaged, and reset may be required.

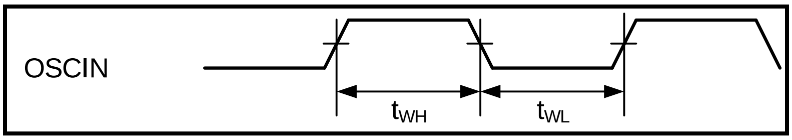

Figure 9: OSCIN Clock Signal

Symbol	Definition	Min	Typ	Max	Units
t_{WH}/t_{WL}	Duty cycle	45		55	%

Table 23: OSCIN Timing

9.5.2 SYSIN

The SYSIN is 125MHz system clock input for interfacing with SyncE PLL. The SYSIN is an optional clock. It can be used for hybrid PTP and SyncE operation. If SYSIN is a valid clock it will be used by the IPC9010 as the reference clock for the clock recovery. In case SYSIN clock is not valid, the core uses OSCIN as reference clock.

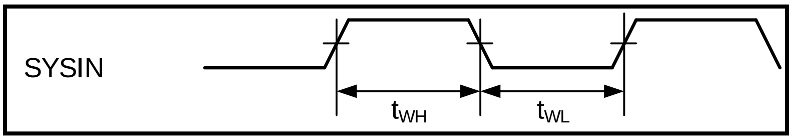

Figure 10: SYSIN Clock Signal

Symbol	Definition	Min	Typ	Max	Units
t_{WH}/t_{WL}	Duty cycle	45		55	%

Table 24: SYSIN Timing

9.5.3 PSCLK

The PSCLK shall be fed by 33.33MHz CXO for CPU operation. PSCLK clock must be valid under all conditions. In case PSCLK will not be valid during IPC9010 operation, the IPC9010 must be reset. For detailed description see Xilinx AC & DC Switching Characteristic Document (DS187).

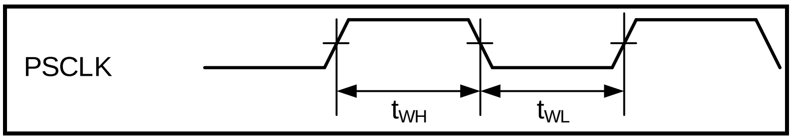

Figure 11: PSCLK Clock Signal

Symbol	Definition	Min	Typ	Max	Units
t_{WH}/t_{WL}	Duty cycle	40		60	%

Table 25: PSCLK Timing

9.5.4 CLKIN

The CLKIN is been used for 1PPS reference clock input in case of PTP master. It's can be also used for APTS (Assisted Partial Timing Support).

9.5.5 Other Clocks

The PPSOUT provides the recovered 1PPS signal. CLKA and CLKB can be used for providing 1PPS to other devices such as PLLs (with 1PPS input) or Ethernet PHY with PTP support.
The CLKOUT provides 1.544MHz, 2.048MHz and 10MHz clock.

9.6 Management UART (mUART) Interface

The mUART interface is for locally configure, control, and monitor the IPC9010 either by external CPU UART interface or from local terminal. The mUART is using standard non-return-to-zero (NRZ) format and is configured to 115,200 baud, 8 bits, No parity, and 1 stop bit.

9.7 Time of Day Interface

The Time of Day interface is comprised of a 1PPS signal and the Time of Day UART providing the NMEA GPRMC message.

Note *The ToD UART will send NMEA messages when in BC or Slave modes only if time is above GPS epoch, i.e., time in parent master is above GPS epoch.*

9.7.1 Time of Day UART (tUART) Interface

The tUART interface is for setting or getting the time-of-day from the IPC9010. When set to operate as IEEE 1588 Master, tUART is for setting the Master time-of-day. When set to operate as IEEE 1588 BC or Slave, tUART is for getting the time-of-day from the IPC9010. The tUART is using standard non-return-to-zero (NRZ) format and is configured to 115,200 baud, 8 bits, No parity, and 1 stop bit.

9.7.2 GPRMC Message Format

The global positioning recommended minimum data (GPRMC) message is a standard national marine electronics association (NMEA) message that provides, amongst other things, UTC date and time. The GPRMC message is supported by all GPS receivers.
When set to Master mode of operation, the IPC9010 is extracting the value from UTC Time field to update the current time. When set to BC or Slave mode of operation, the IPC9010 is transmitting GPRMC messages.

The IPC9010 GPRMC output message (62 bytes) format is given in the following example:

$GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0,0.0,110410,,,A*66

The IPC9010 supports two GPRMC input messages formats:

$GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0,0.0,110410,,,A*66
$GPRMC,122356.00,A,3523.414,N,13932.106,W,,,110410,,,A*43

The IPC9010 GPRMC output message is described in Table 26 below.

Field	Description
Message ID	$GPRMC
UTC Time	122356 (hh:mm:ss)
Status	A – Data valid or V – Data invalid
Latitude	0000.0000 (fixed to zero)
N/S Indicator	N- North
Longitude	0000.0000 (fixed to zero)
E/W Indicator	W – West
Speed over Ground	0.0 (fixed to zero)
Course over Ground	0.0 (fixed to zero)

Field	Description
UTC Date	110410 (ddmmyy)
Magnetic Variation	Empty
Direction of Variation	Empty
Mode	A = autonomous
Checksum	*66

Table 26: GPRMC Output Message Format using tUART

9.7.3 Timing Diagrams

The ToD input is comprised of the tUART TURX pin and a reference PPS signal connected to CLKIN pin. Figure 12 below depicts the TURX and CLKIN signals timing.

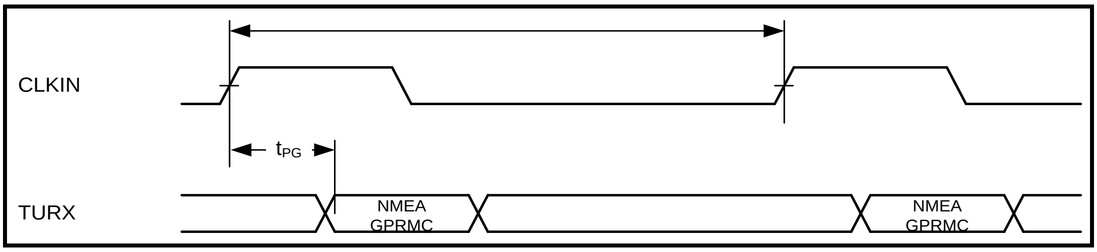

Figure 12: CLKIN and TURX Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{PG}	Time between PPSIN rising edge and GPRMC message	0.5		200	ms

Table 27: CLKIN and TURX Timing Table

The ToD output is comprised of the tUART TUTX pin and the PPSOUT pin. Figure 13 below depicts the TUTX and PPSOUT signals timing.

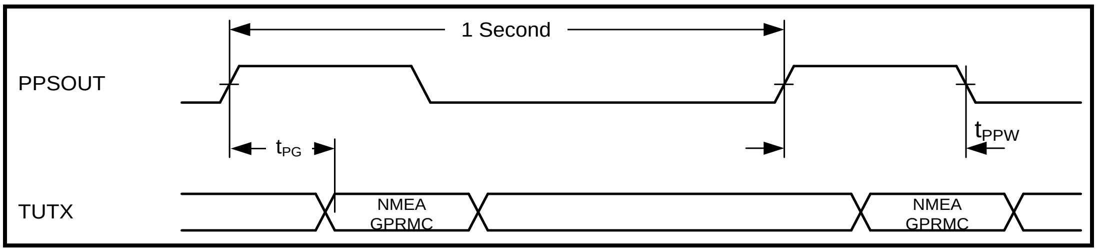

Figure 13: PPSOUT and TUTX Timing Diagram

Symbol	Definition	Min	Typ	Max	Units
t_{PG}	Time between PPSOUT rising edge and GPRMC message	0.5		200	ms
t_{PPW}	PPSOUT pulse width	200	250	300	ms

Table 28: PPSOUT and TUTX Timing Table

9.8 Status Interface

The status interface includes the following: STAT[1:0], STATFR, STATTR, STATLK and STATHO pins.
Table 14 below defines the IPC9010 STAT[1:0] pins truth table.

STAT[1:0]	State	
00	Fail:	Core is not operating as required
01	Alarm:	Core may not operate as required or it is not in lock state
10	Pass:	Core is operating as required and it is in lock state

Table 29: STAT[1:0] Pins Truth Table

For additional information about STAT[1:0], see administrative state-machine chapter.
For detailed information about STATFR, STATTR, STATLK and STATHO, see core state-machine chapter.

10 Ordering Information

Symbol	Definition
IPC9010	IEEE 1588 BC/Slave/Master IP core

11 Contact Information

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